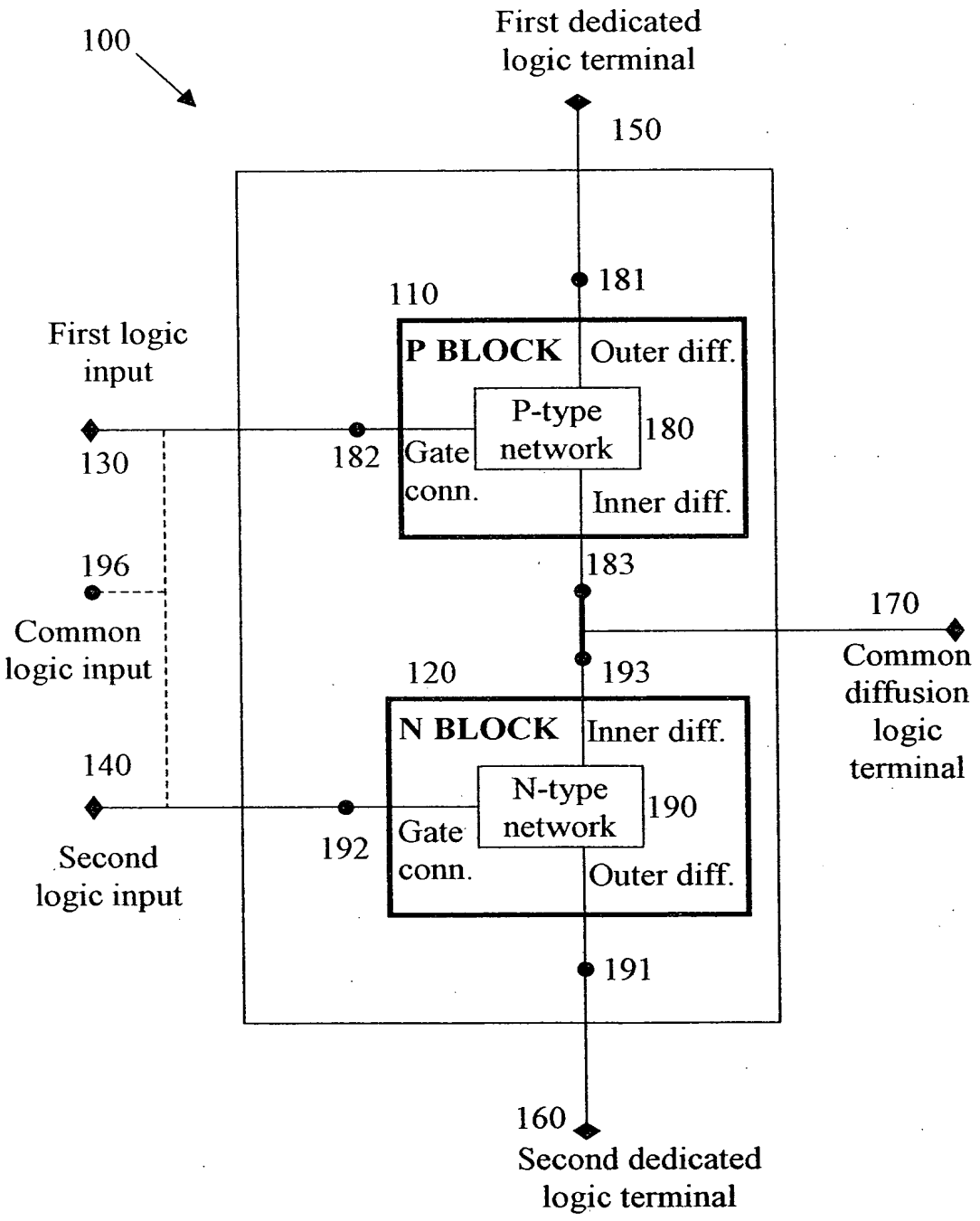


Fig. 1

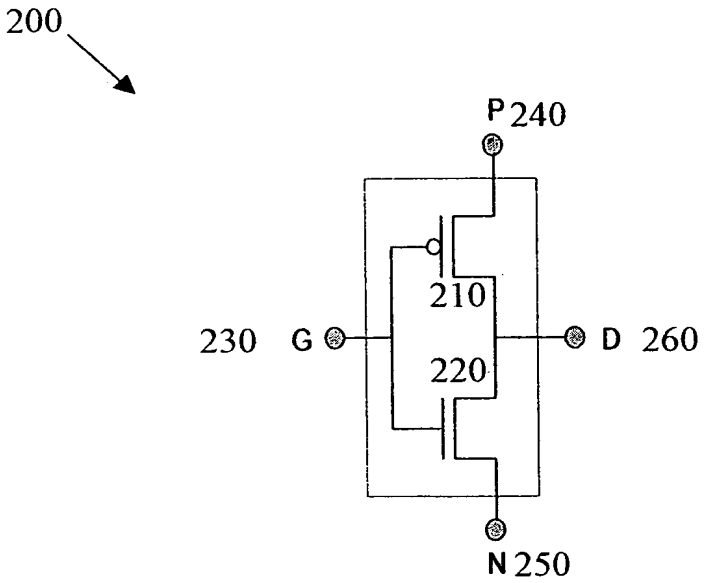

200
P 240
210
230 G
D 260
220
N 250

Fig. 2

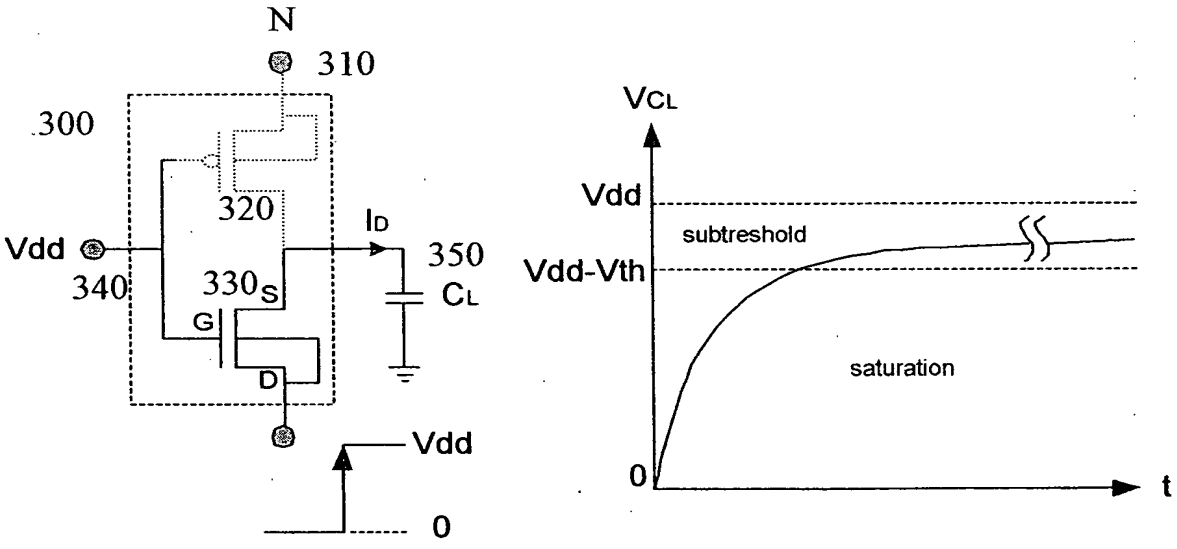

N
310
300
320
Vdd
340
330S
G
D
ID
350
CL
Vdd
0
VCL
Vdd
subtreshold
Vdd-Vth
saturation
0
t

Fig. 3

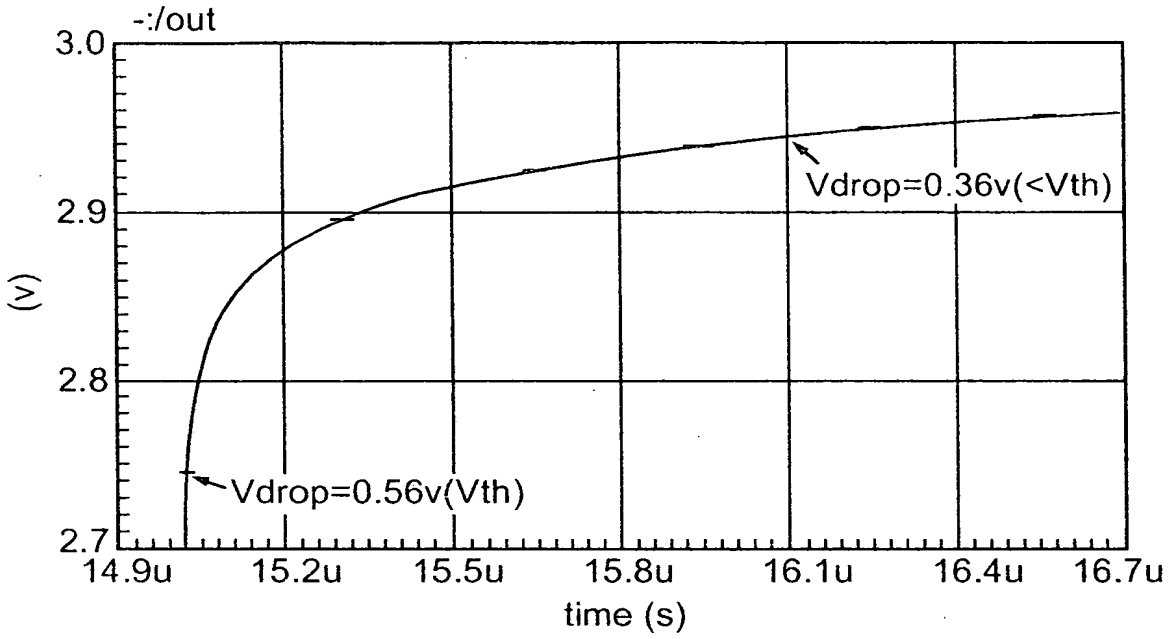

-:/out
3.0
2.9
2.8
2.7
(v)
Vdrop=0.36v(<Vth)
Vdrop=0.56v(Vth)
14.9u
15.2u
15.5u
15.8u
16.1u
16.4u
16.7u
time (s)

Fig. 4

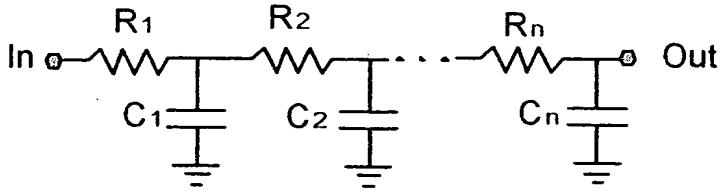

R1
R2
Rn
In
Out
C1
C2
Cn

Fig. 5

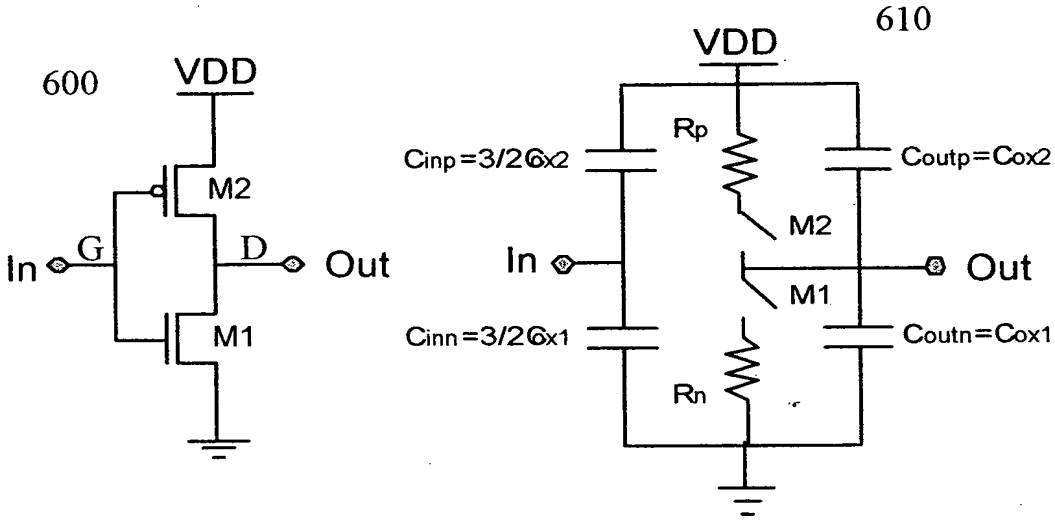

600
VDD
M2
In
G
D
Out
M1
610
VDD
Rp
Cinp=3/26x2
Coutp=Cox2
M2
In
Out
M1
Cinn=3/26x1
Coutn=Cox1
Rn

Fig. 6

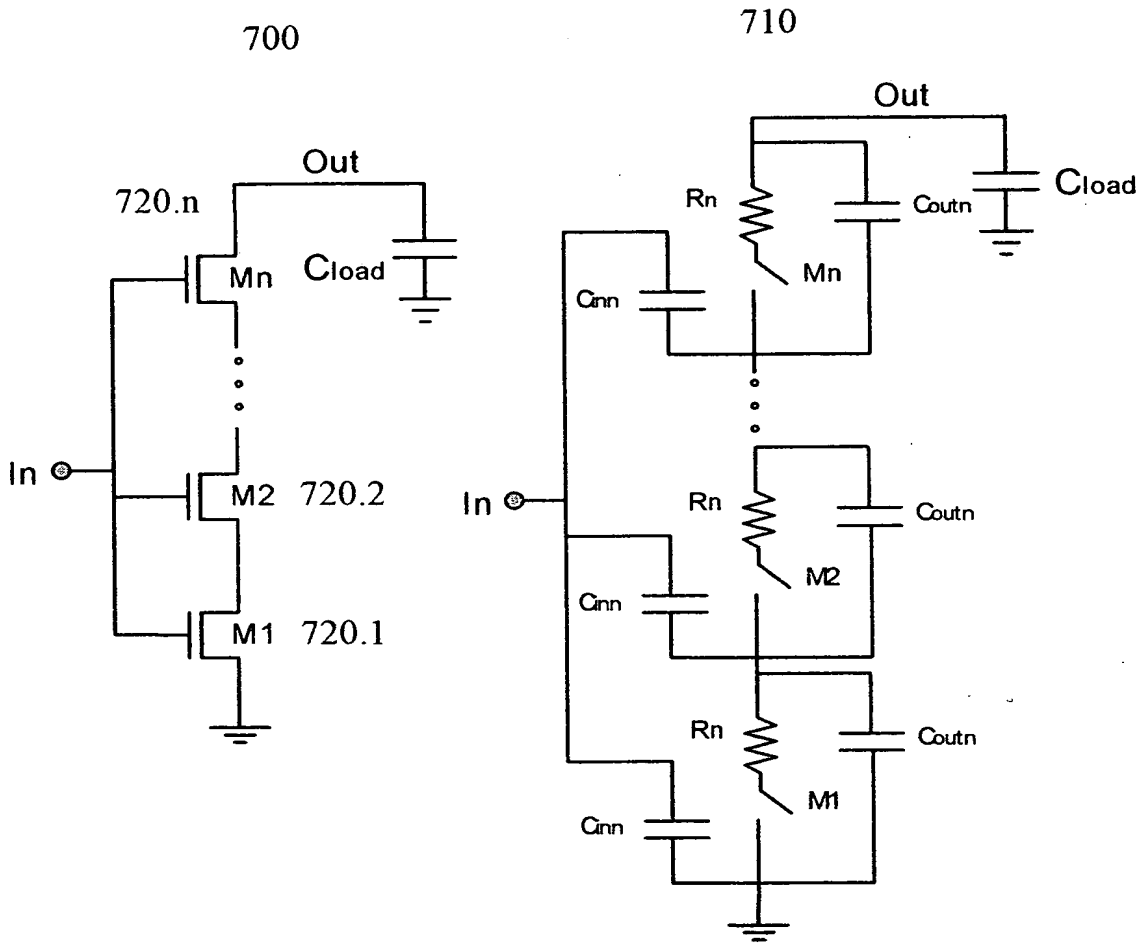


Fig. 7 - Prior art

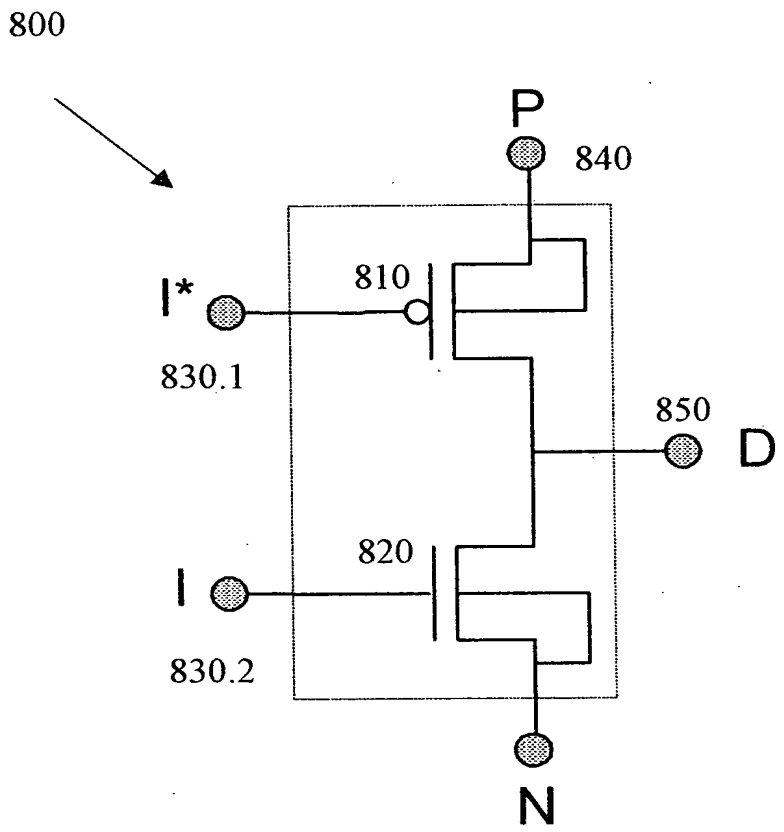


Fig. 8

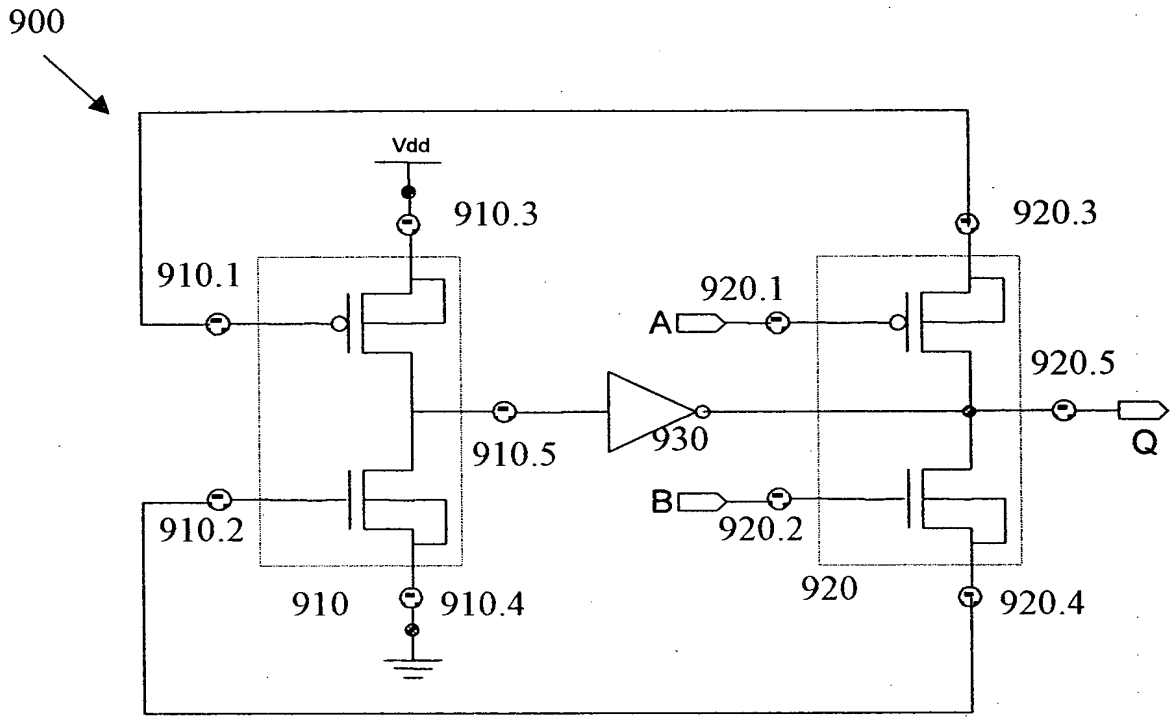

900
Vdd
910.3
910.1
920.3
920.1
A
920.5
910.5
930
Q
910.2
B
920.2
910
910.4
920
920.4

Fig. 9

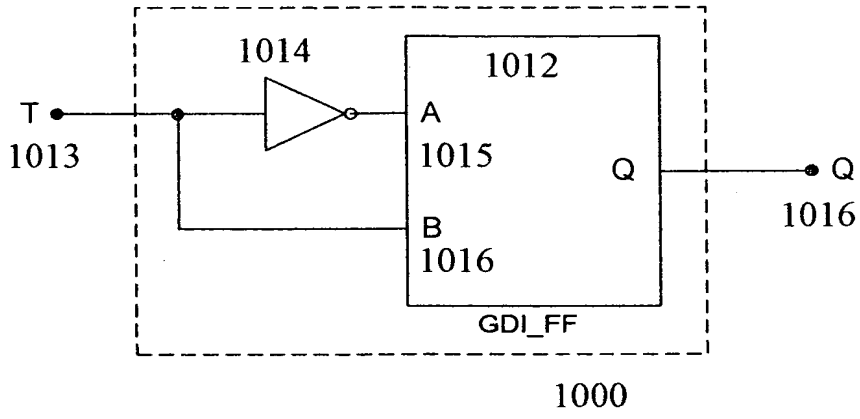


Fig. 10a

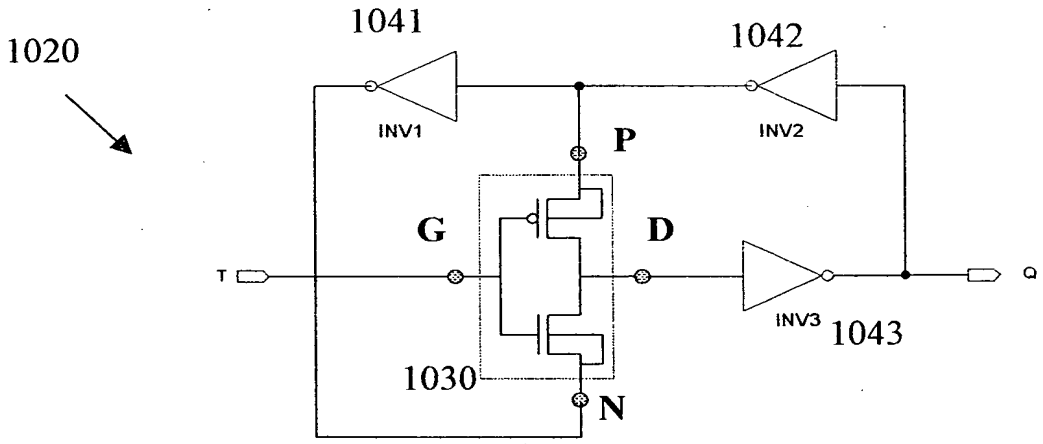


Fig. 10b

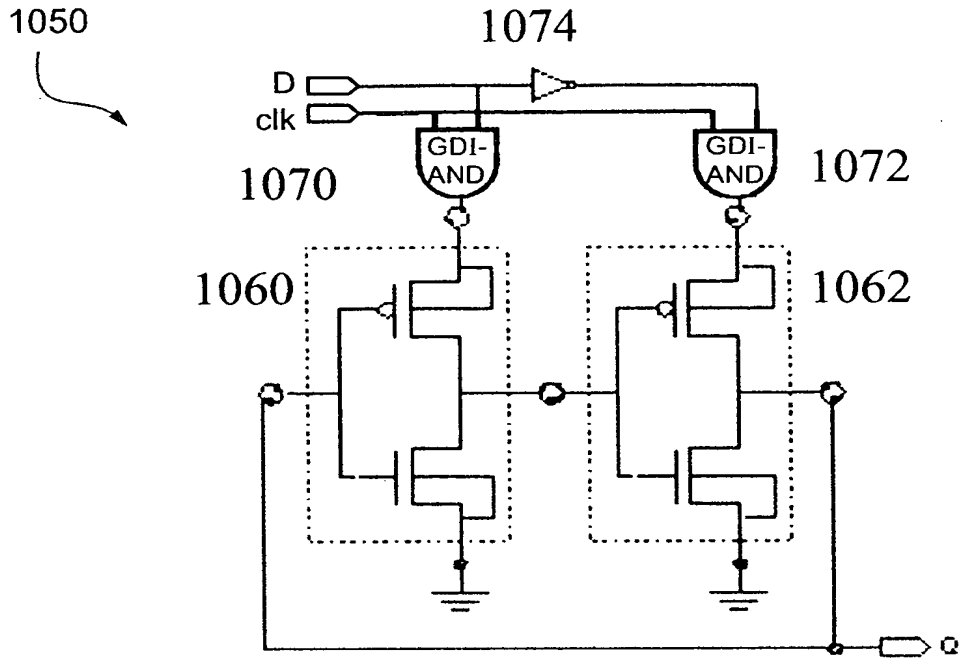


Fig. 10c

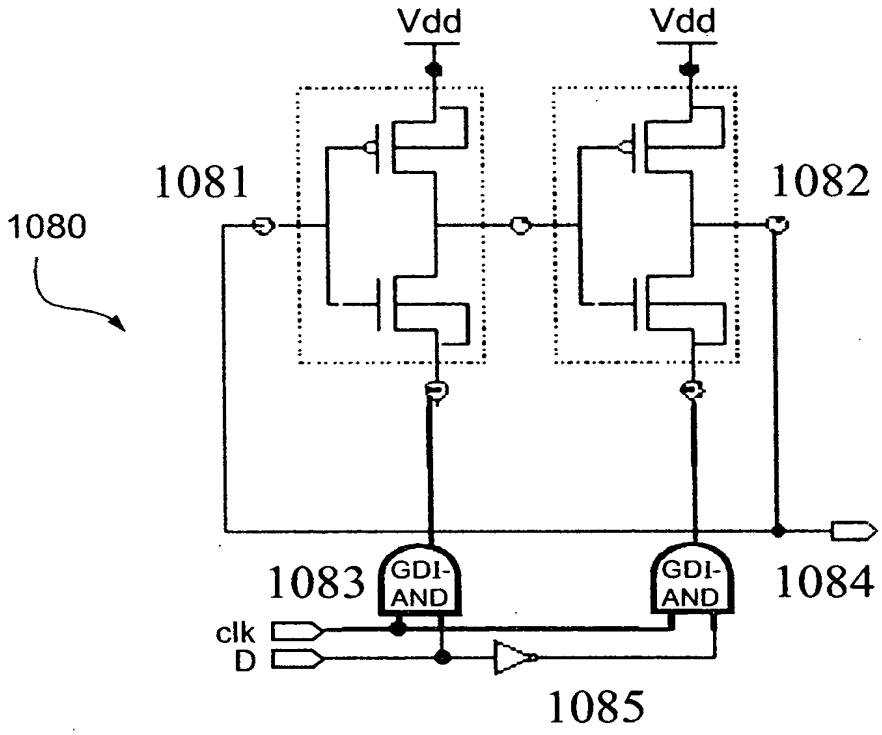


Fig. 10d

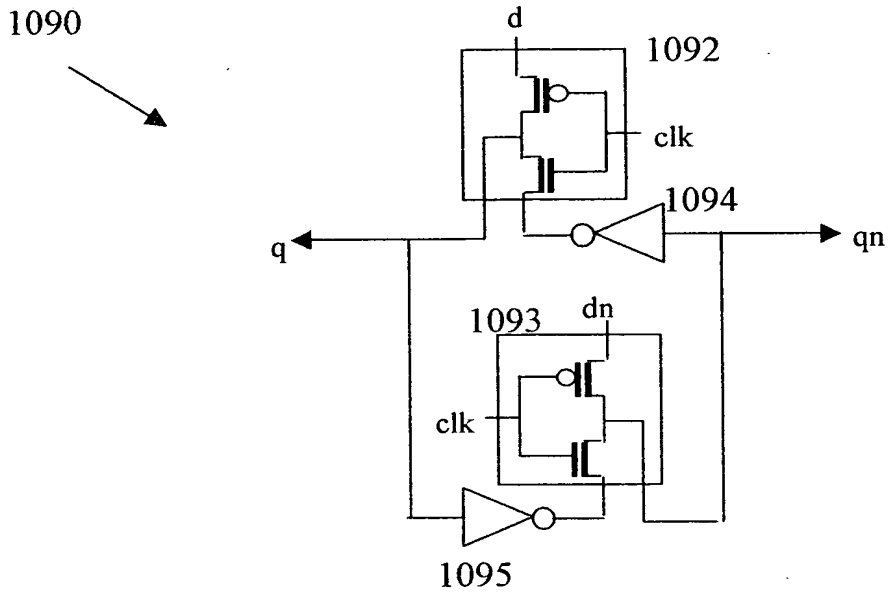


Fig. 10e

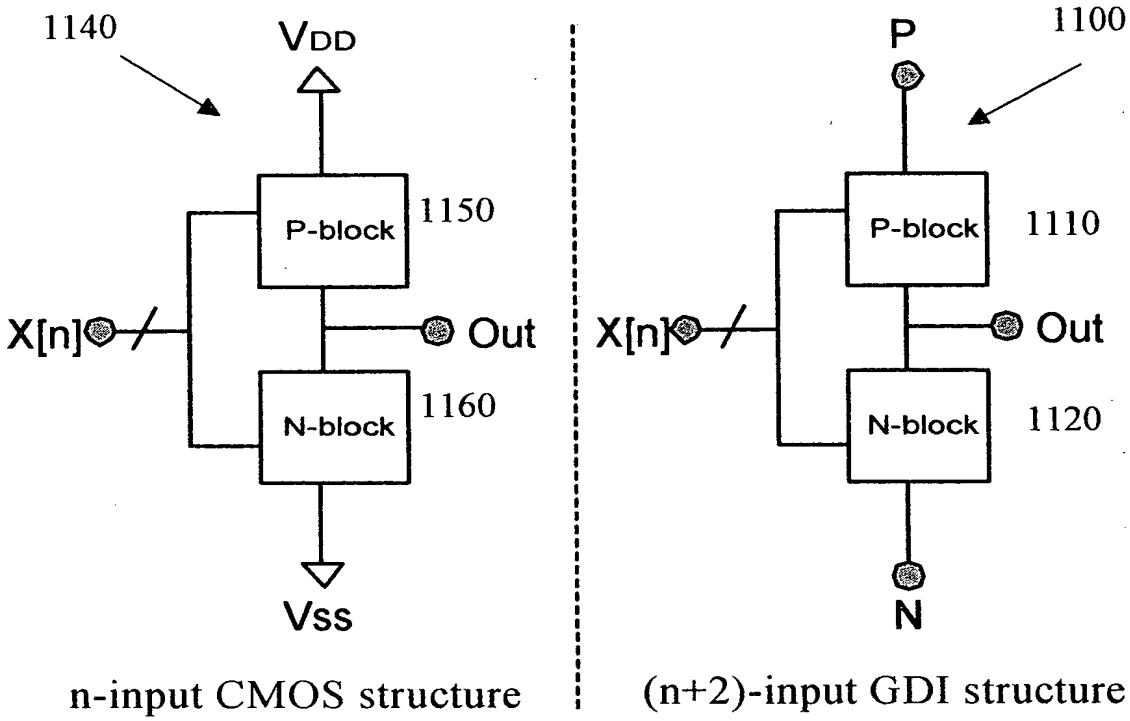
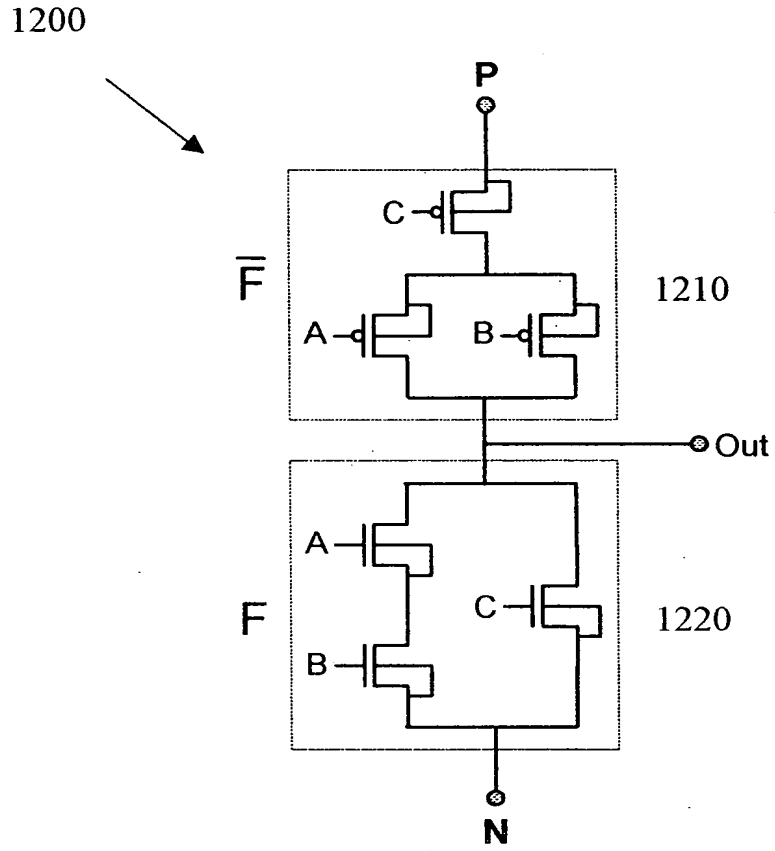

1140
VDD
P-block
1150
X[n]
Out
N-block
1160
Vss
n-input CMOS structure
P
1100
P-block
1110
X[n]
Out
N-block
1120
N
(n+2)-input GDI structure

Fig. 11



$$Out=\overline{F}P+FN=\overline{(AB+C)}P+(AB+C)N$$

Fig. 12

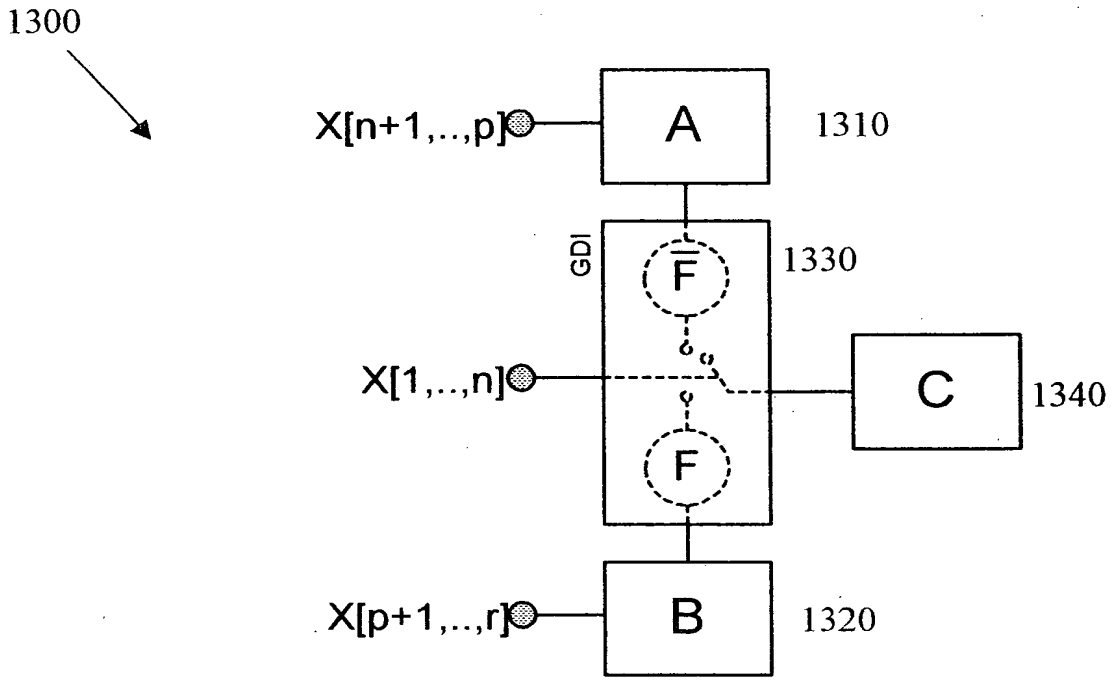


Fig. 13

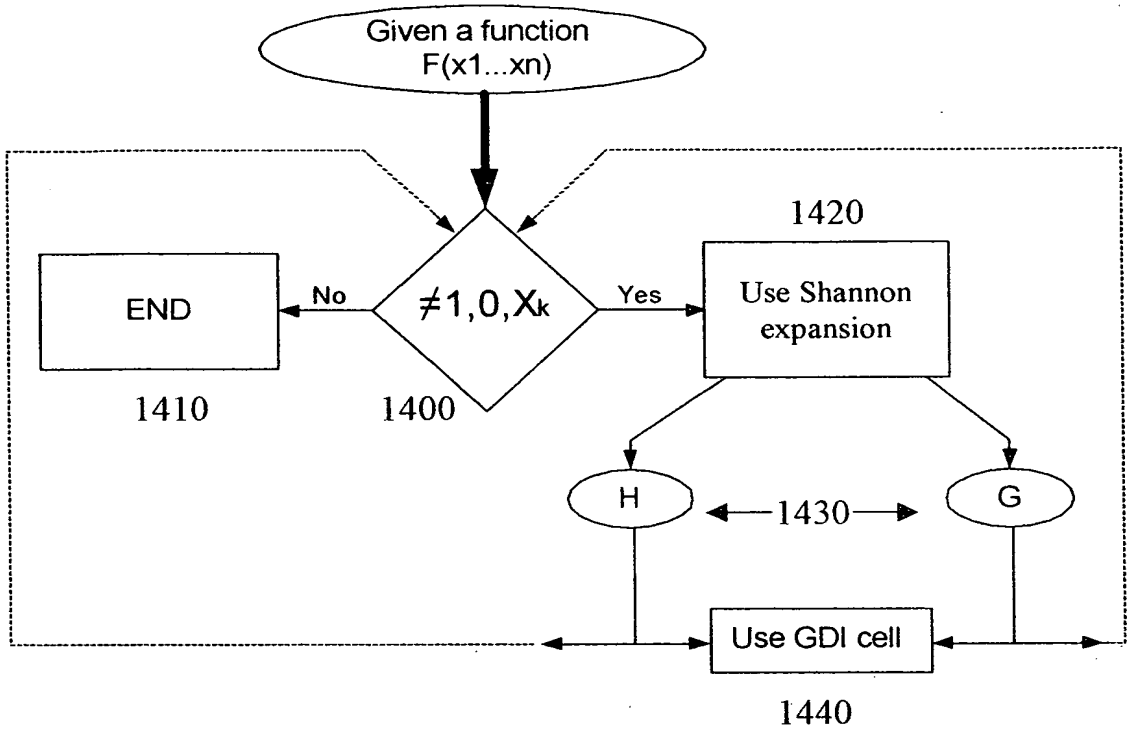

Given a function
F(x1...xn)
1420
END
No
≠1,0,Xk
Yes
Use Shannon
expansion
1410
1400
H
1430
G
Use GDI cell
1440

Fig. 14

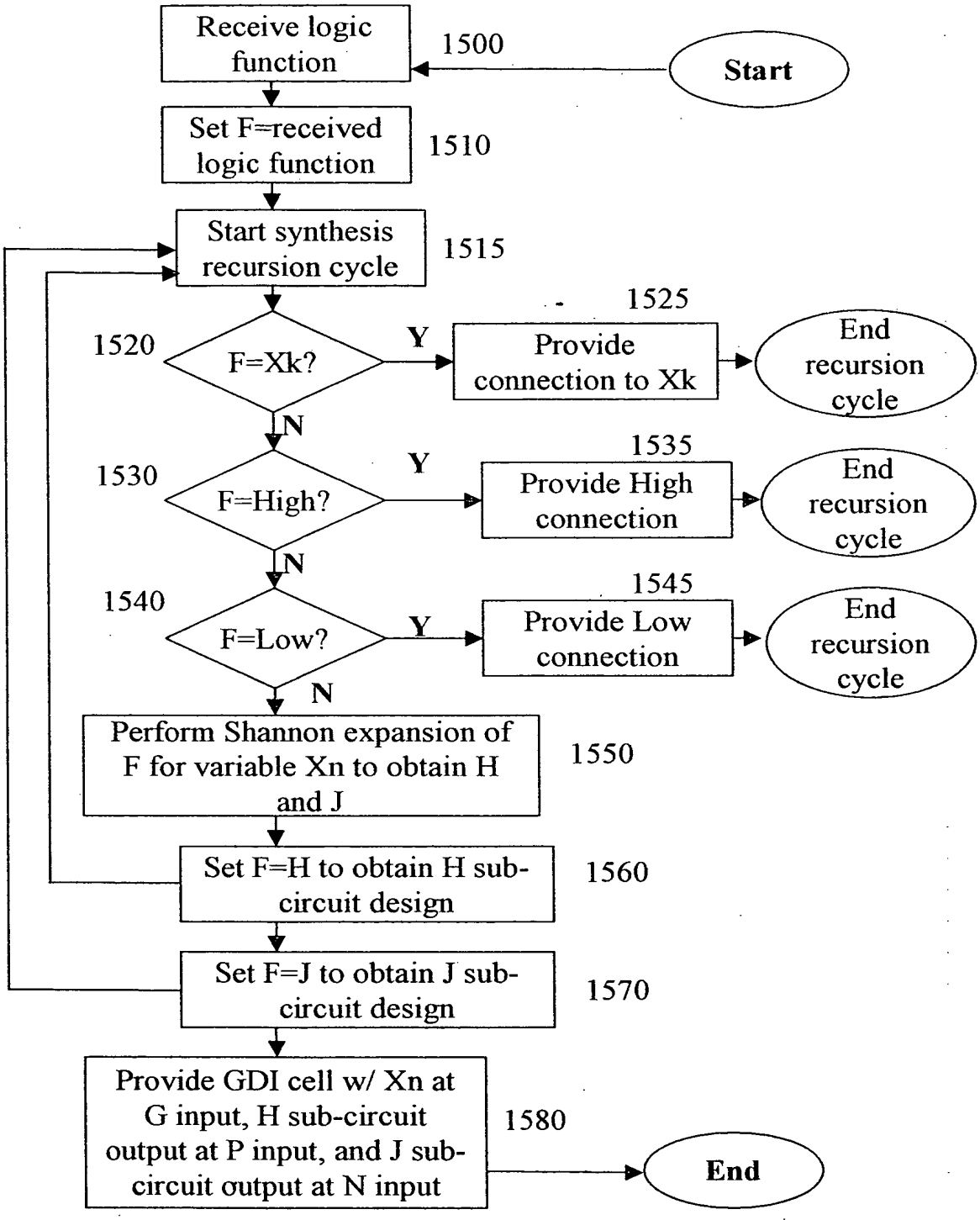

Start
Receive logic function
1500
Set F=received logic function
1510
Start synthesis recursion cycle
1515
F=Xk?
1520
Y
Provide connection to Xk
1525
End recursion cycle
N
F=High?
1530
Y
Provide High connection
1535
End recursion cycle
N
F=Low?
1540
Y
Provide Low connection
1545
End recursion cycle
N
Perform Shannon expansion of F for variable Xn to obtain H and J
1550
Set F=H to obtain H sub-circuit design
1560
Set F=J to obtain J sub-circuit design
1570
Provide GDI cell w/ Xn at G input, H sub-circuit output at P input, and J sub-circuit output at N input
1580
End

Fig. 15

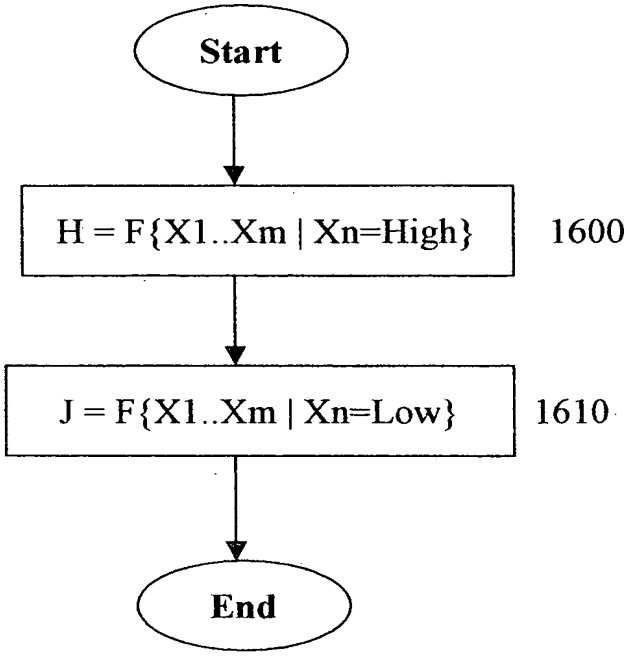


Fig. 16

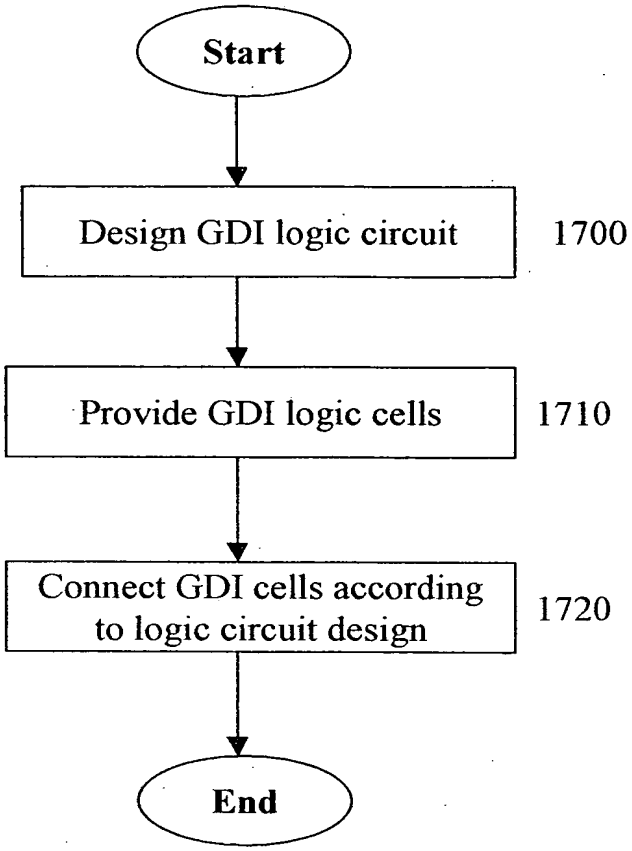
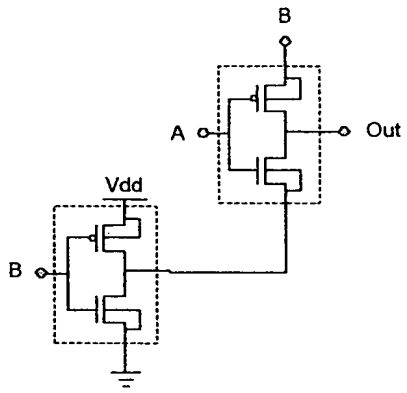
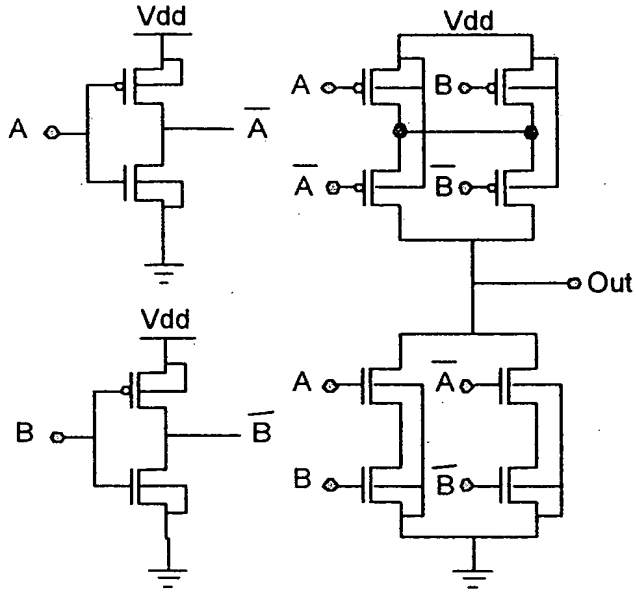

Start
Design GDI logic circuit
1700
Provide GDI logic cells
1710
Connect GDI cells according to logic circuit design
1720
End

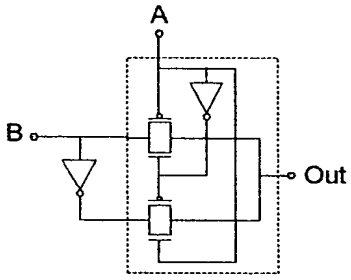
Fig. 17



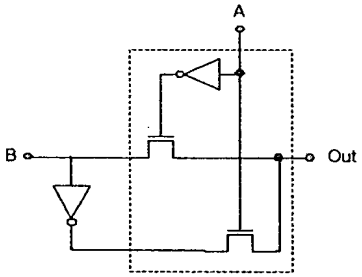
GDI
4 transistors



CMOS – Prior art
12 transistors



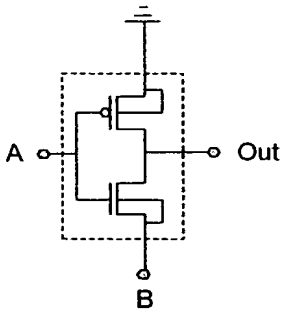
TG – Prior art
8 transistors



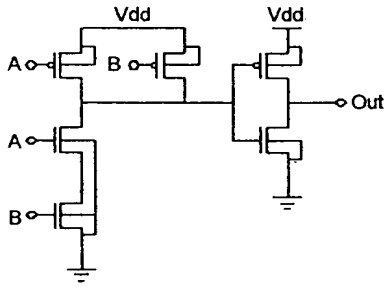
N-PG – Prior art
6 transistors

XOR gate

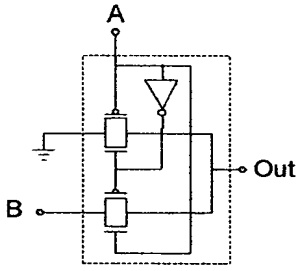
Fig. 18a



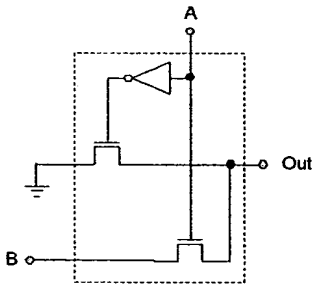
GDI
2 transistors



CMOS - Prior art
6 transistors



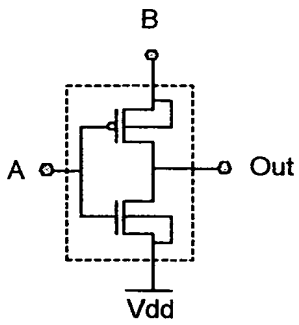
TG - Prior art
6 transistors



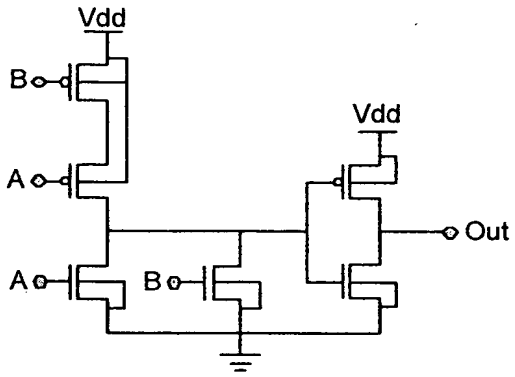
N-PG - Prior art
4 transistors

AND gate

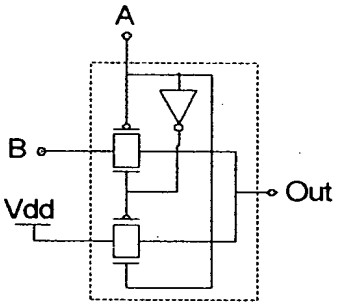
Fig. 18b



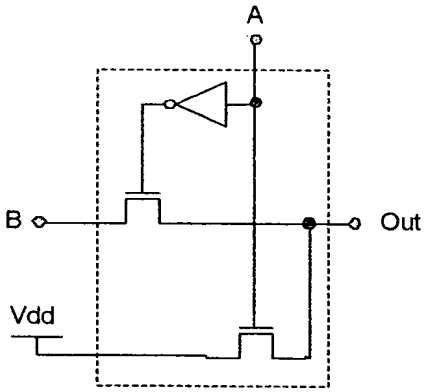
GDI
2 transistors



CMOS - Prior art
6 transistors



TG - Prior art
6 transistors



N-PG - Prior art
4 transistors

OR gate

Fig. 18c

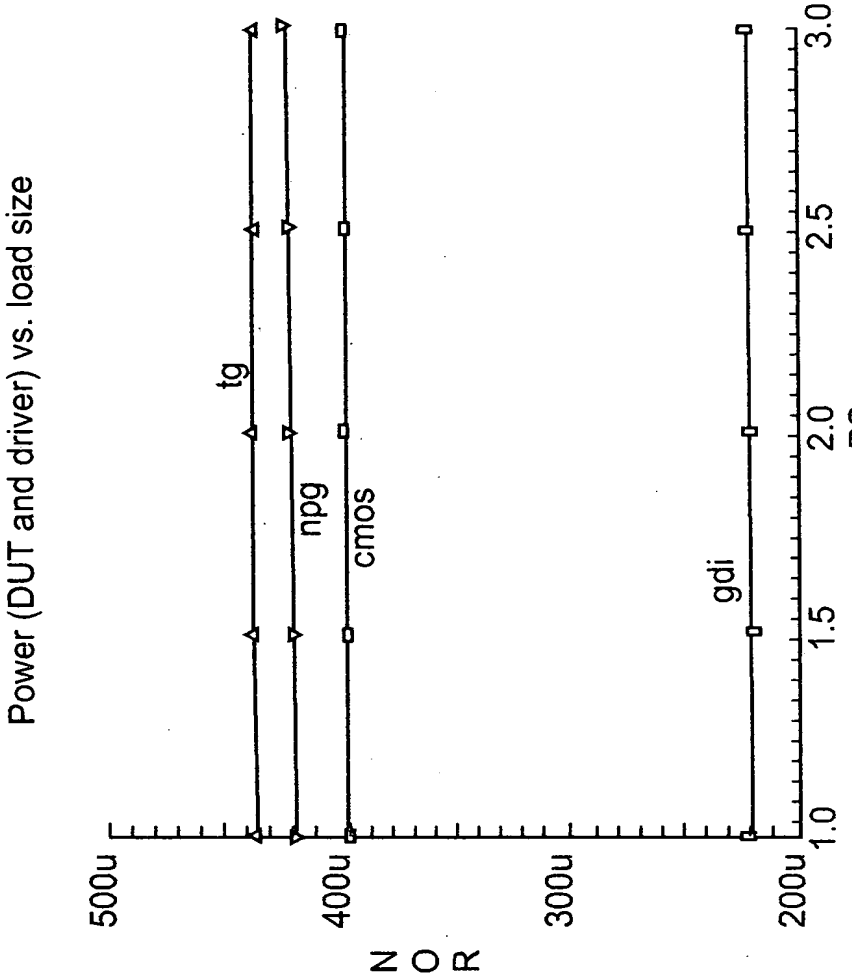


Fig. 19b

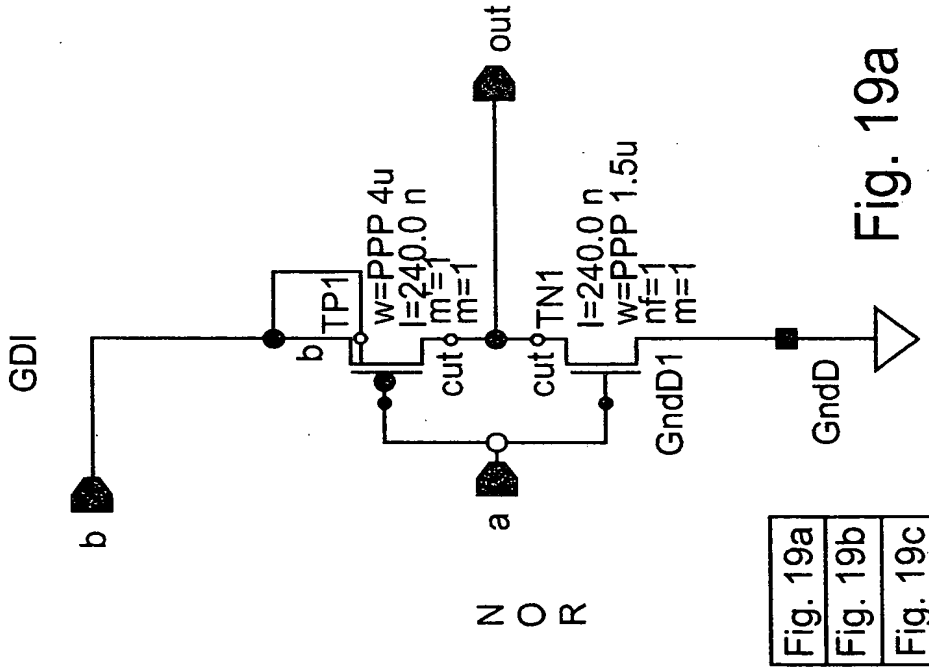


Fig. 19a

Fig. 19a	Fig. 19b	Fig. 19c	Fig. 19d	Fig. 19e	Fig. 19f

Fig. 19

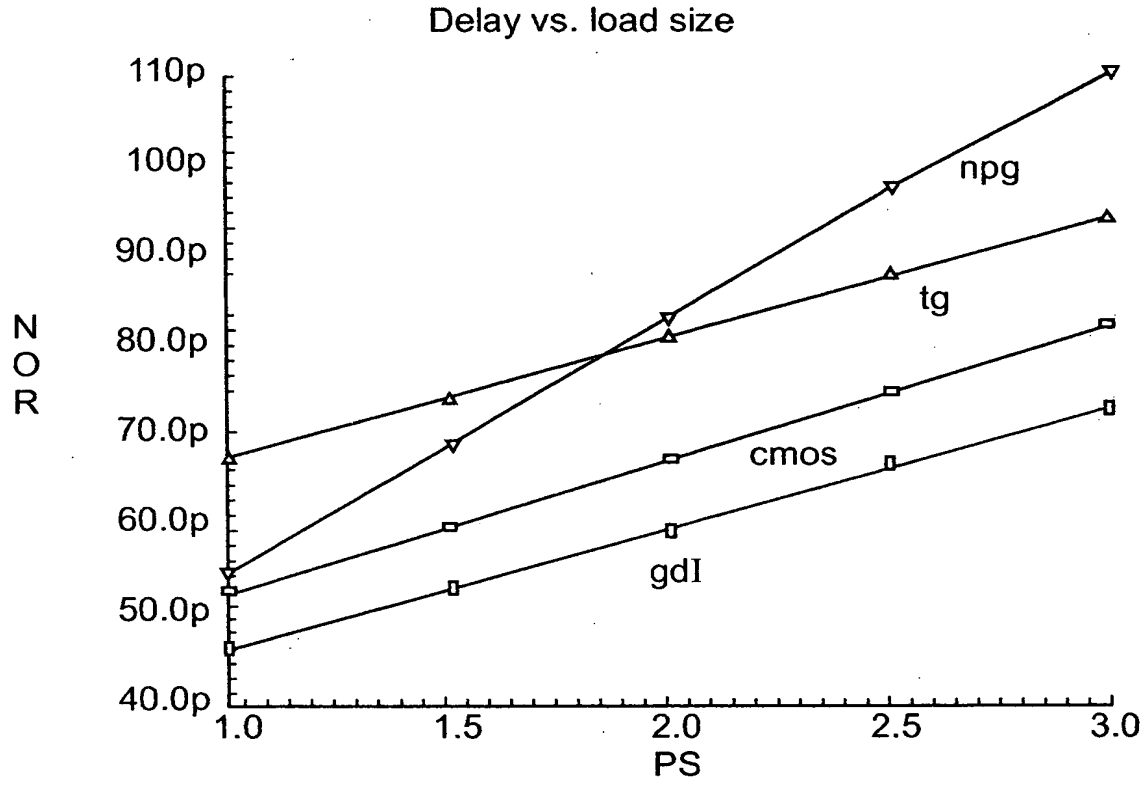

Delay vs. load size
110p
100p
90.0p
80.0p
70.0p
60.0p
50.0p
40.0p
NOR
1.0
1.5
2.0
2.5
3.0
PS
npg
tg
cmos
gdI

Fig. 19c

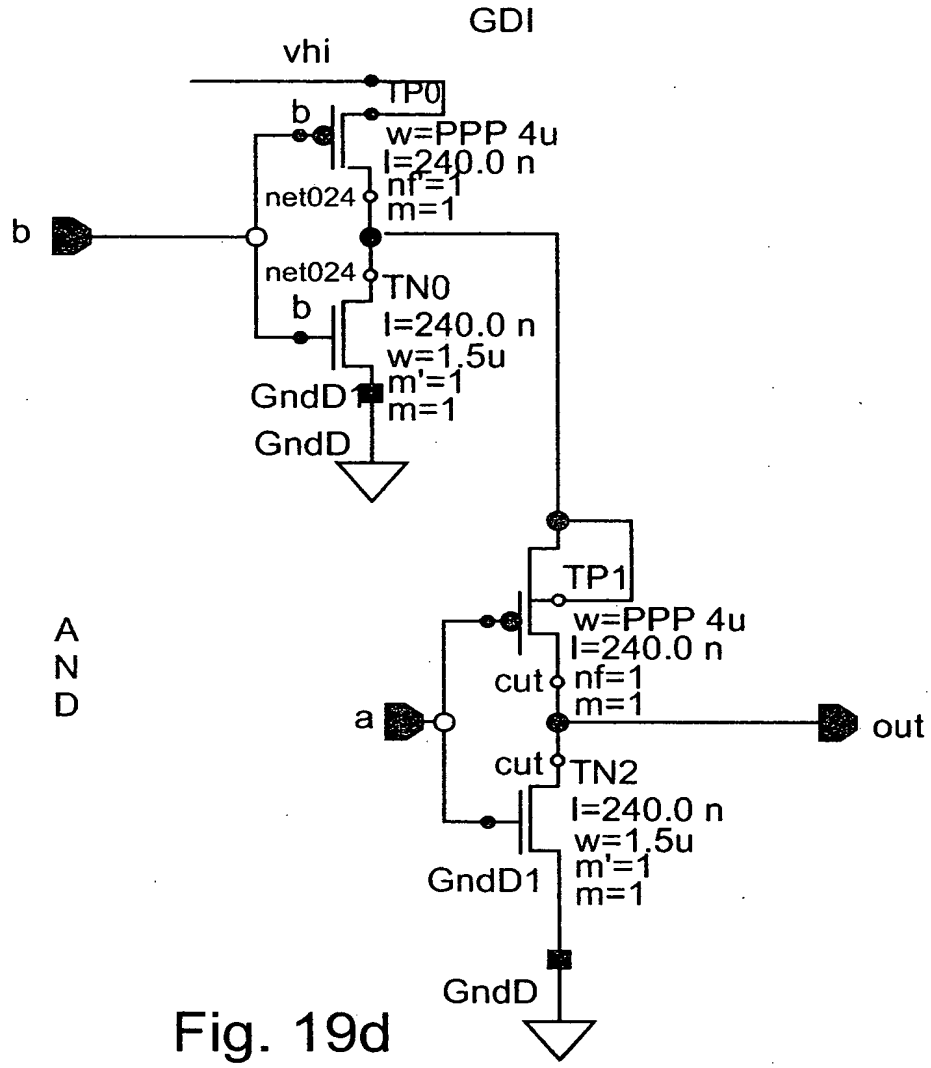

GDI
vhi
TP0
b
w=PPP 4u
l=240.0 n
nf=1
m=1
net024
b
net024
TN0
b
l=240.0 n
w=1.5u
m'=1
m=1
GndD1
GndD
TP1
w=PPP 4u
l=240.0 n
cut
nf=1
m=1
a
out
cut
TN2
l=240.0 n
w=1.5u
m'=1
m=1
GndD1
GndD
A
N
D

Fig. 19d

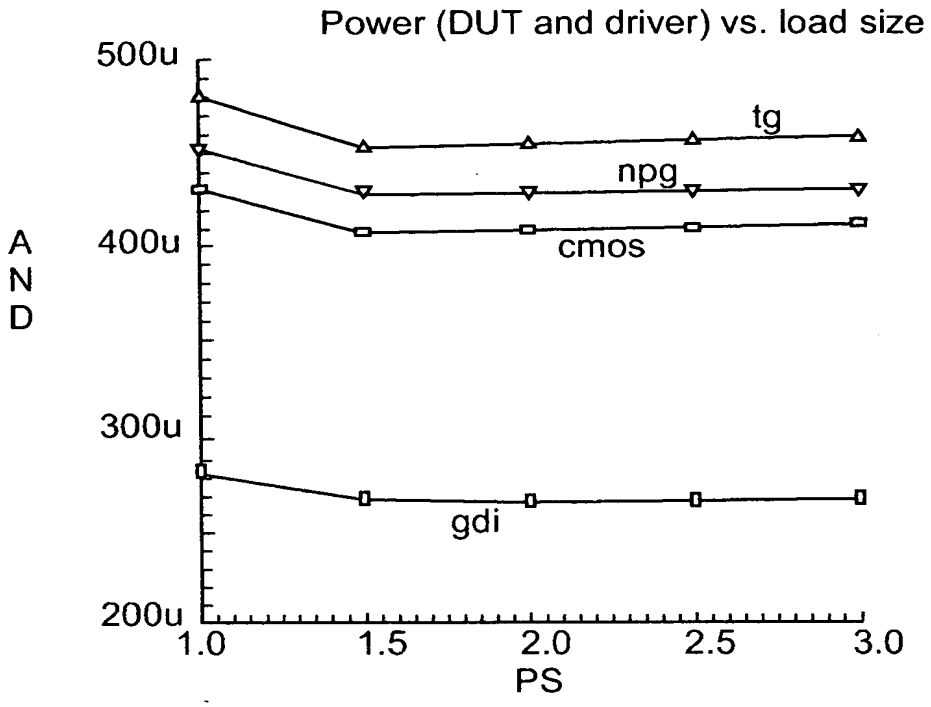


Fig. 19e

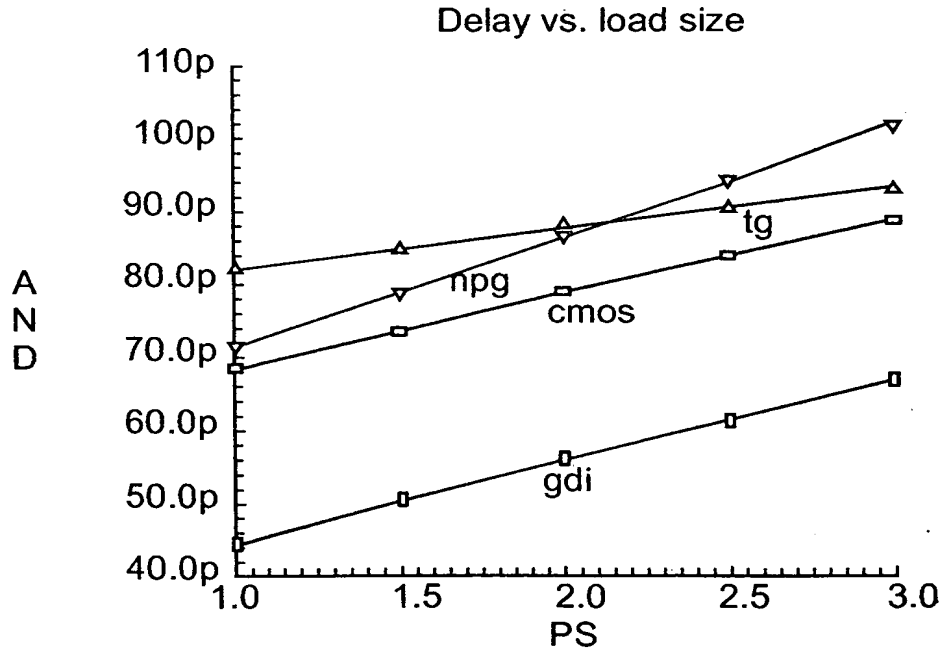


Fig. 19f

Fig. 20a
Fig. 20b
Fig. 20c
Fig. 20d
Fig. 20e
Fig. 20f

Fig. 20

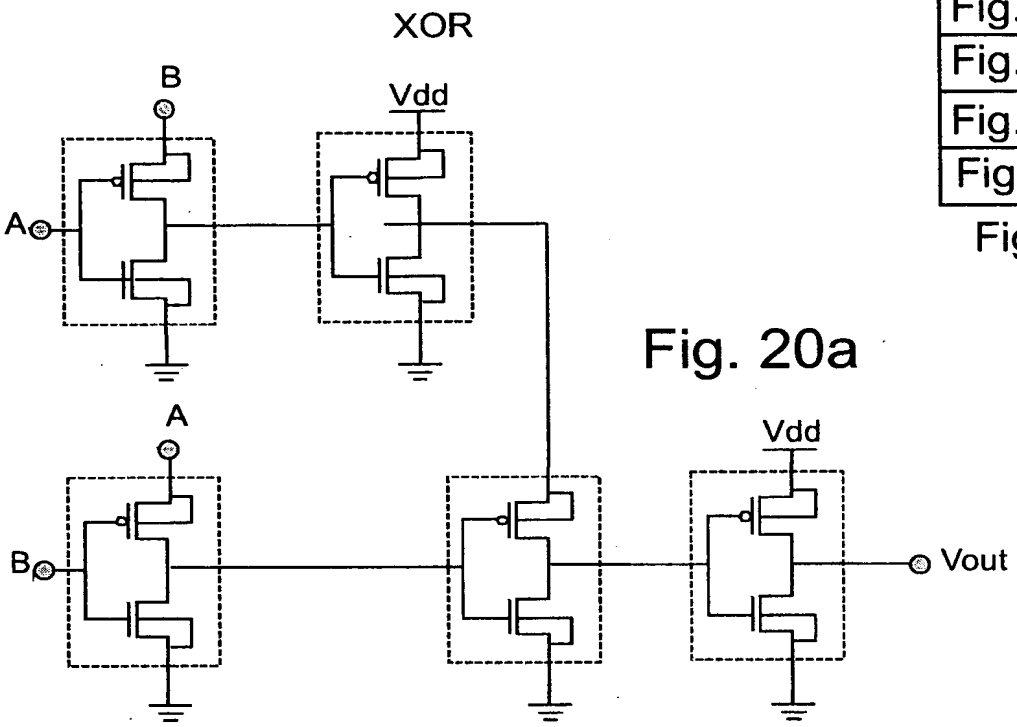


Fig. 20a

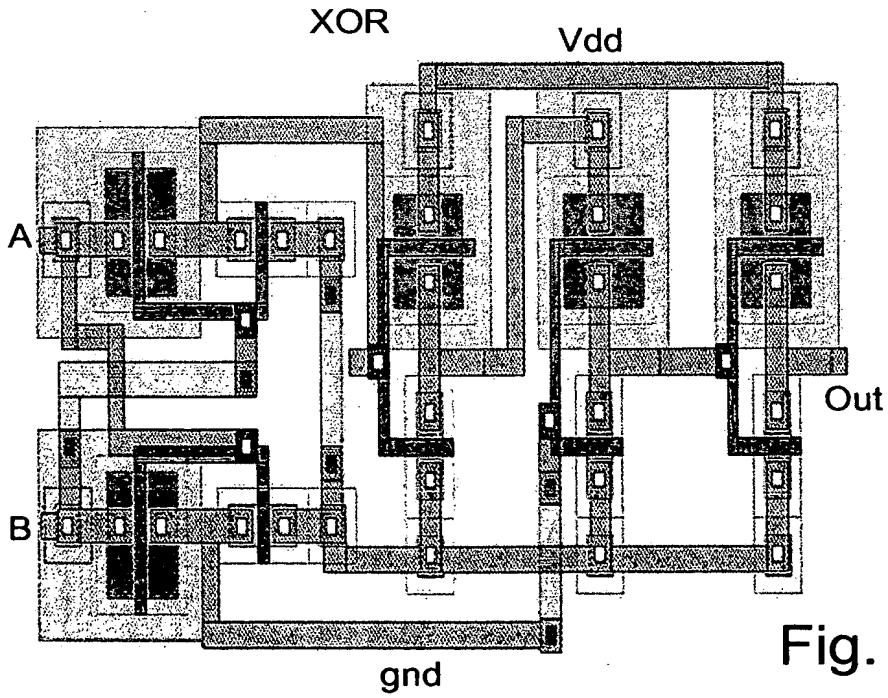


Fig. 20b

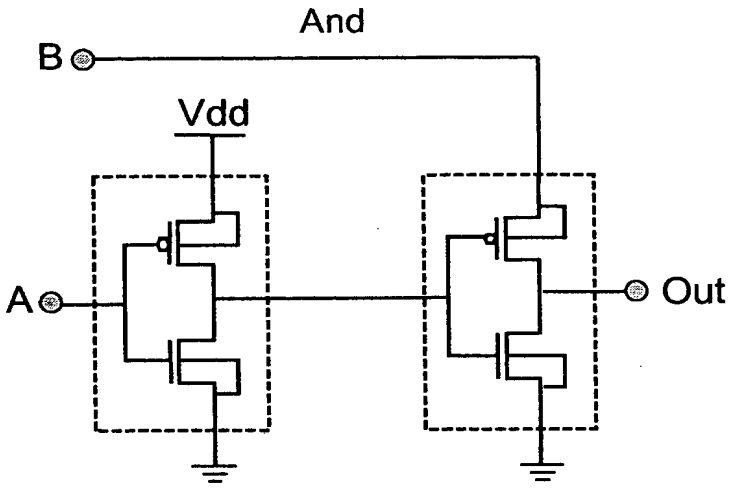


Fig. 20c

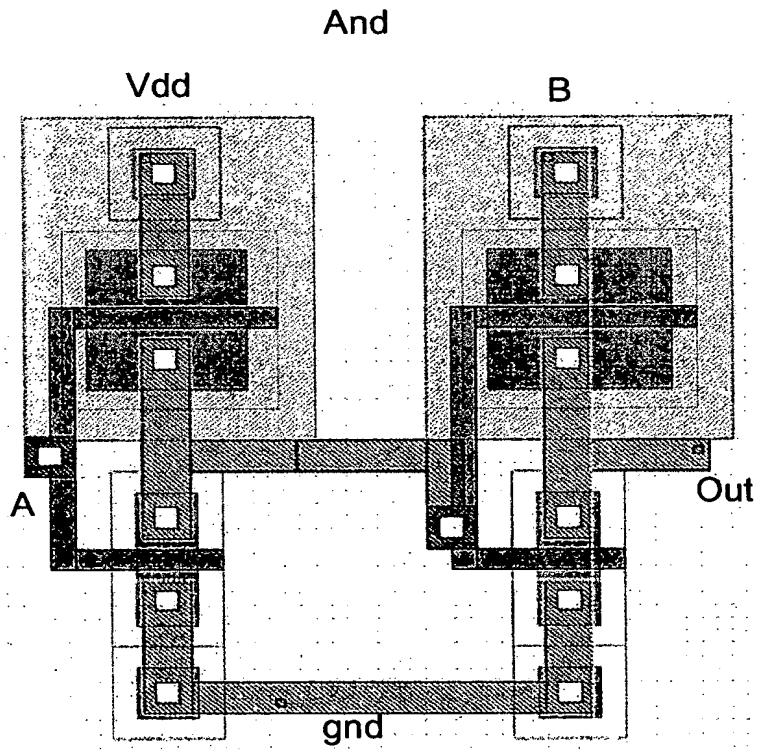


Fig. 20d

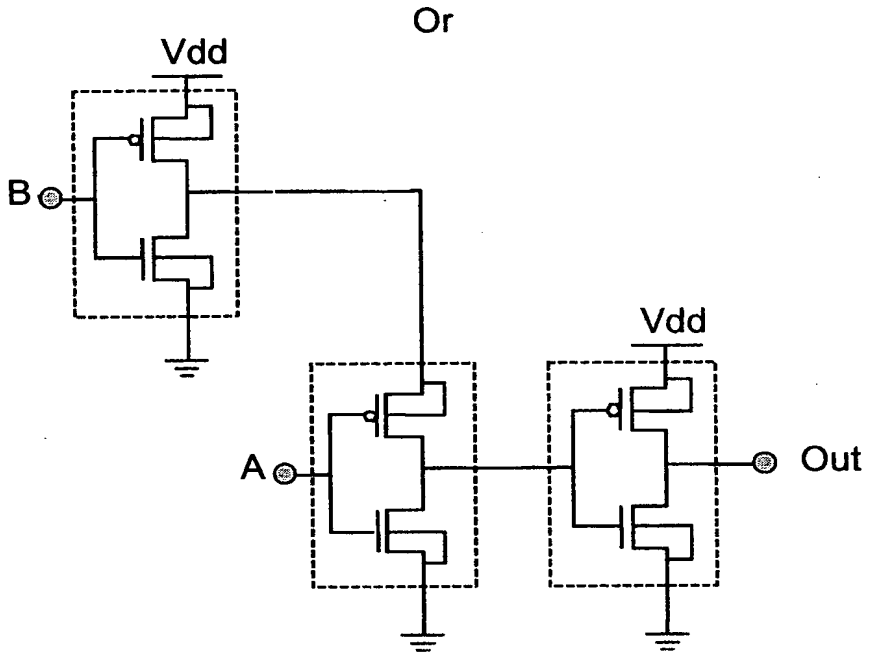


Fig. 20e

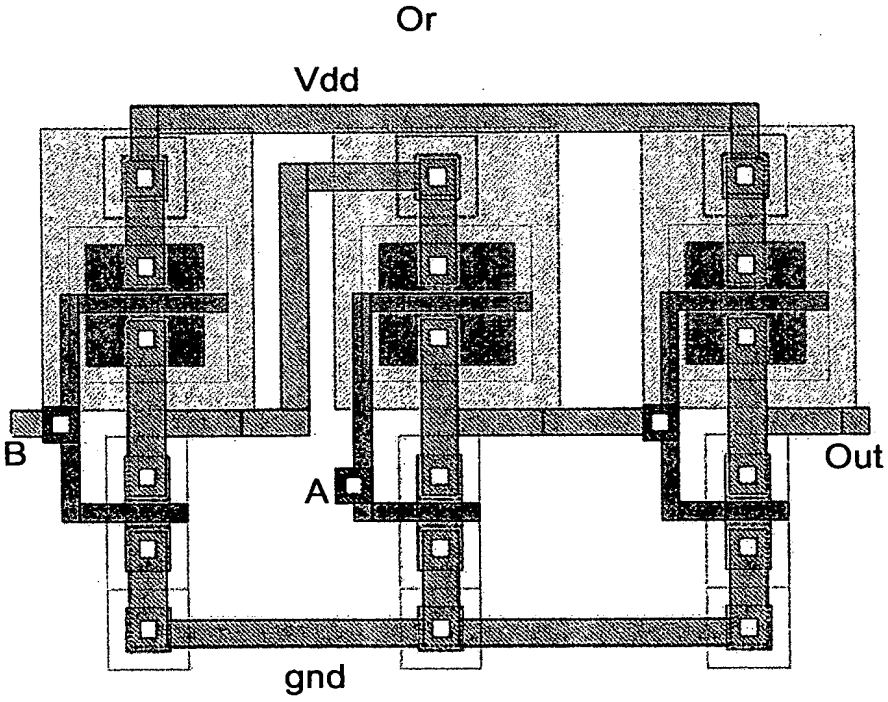
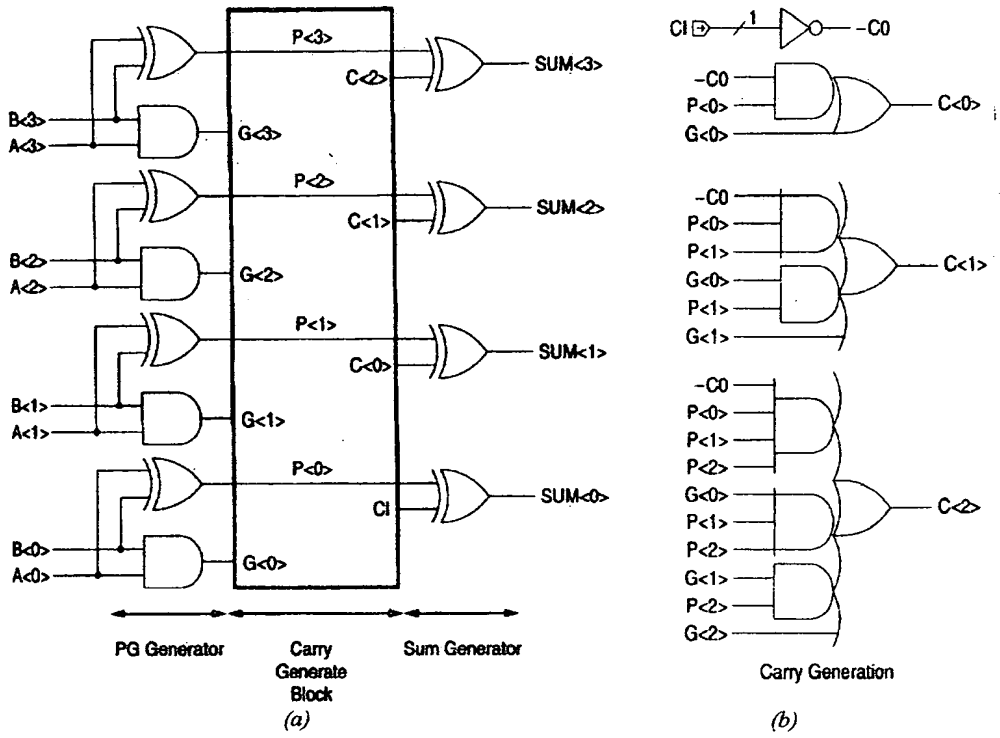


Fig. 20f



a) Basic scheme

b) Carry Generator (3-bit only)

Fig. 21 – Prior art

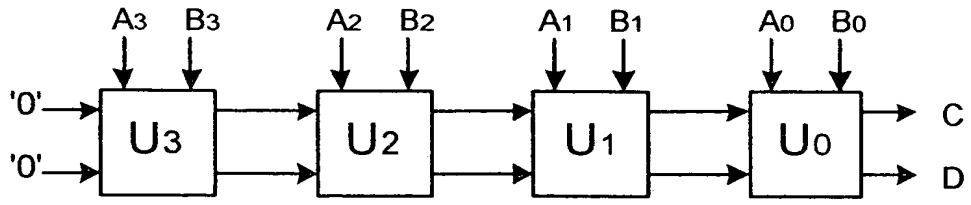


Fig. 22 – Prior art

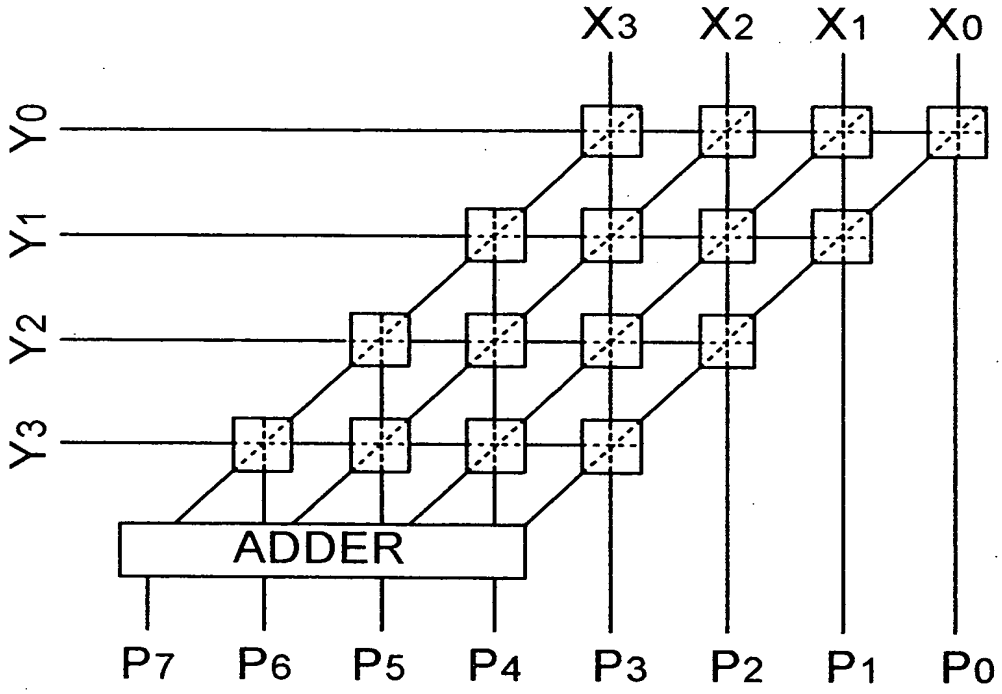


Fig. 23 – Prior art

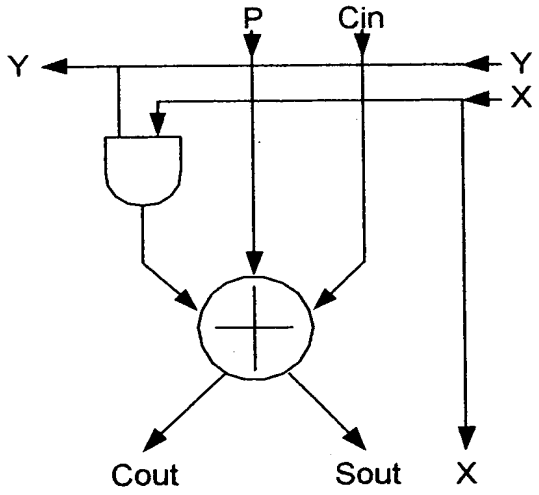
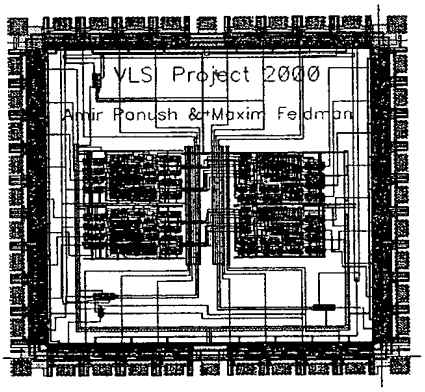
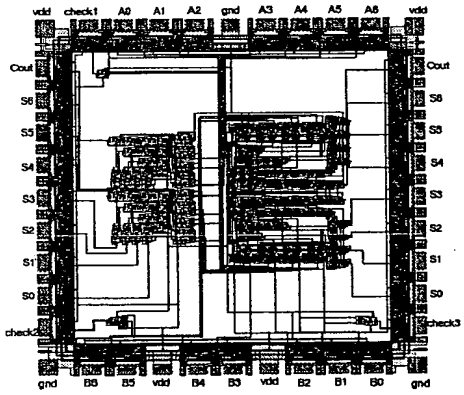


Fig. 24 – Prior art





a) GDI and prior art CMOS

b) GDI and prior art TG

Fig. 25

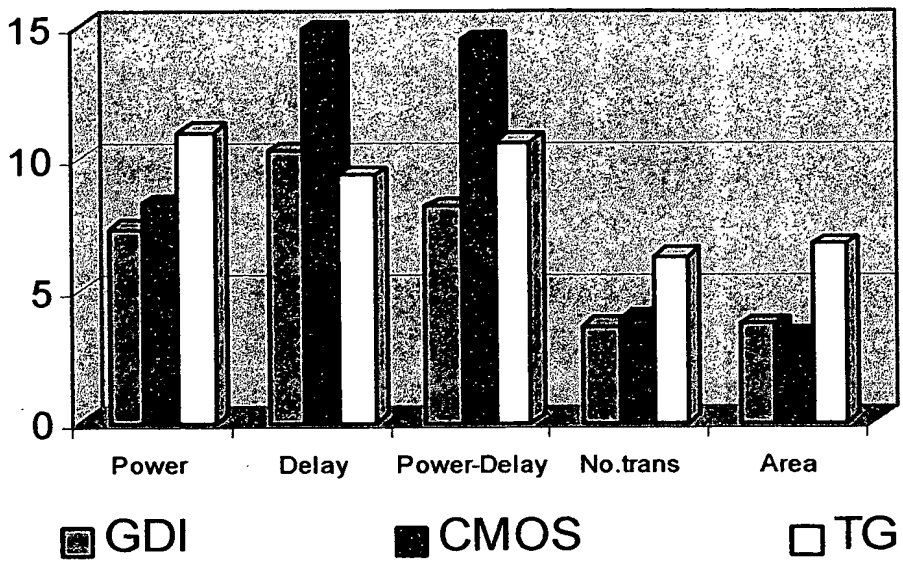

15
10
5
0
Power
Delay
Power-Delay
No.trans
Area
GDI
CMOS
TG

Fig. 26

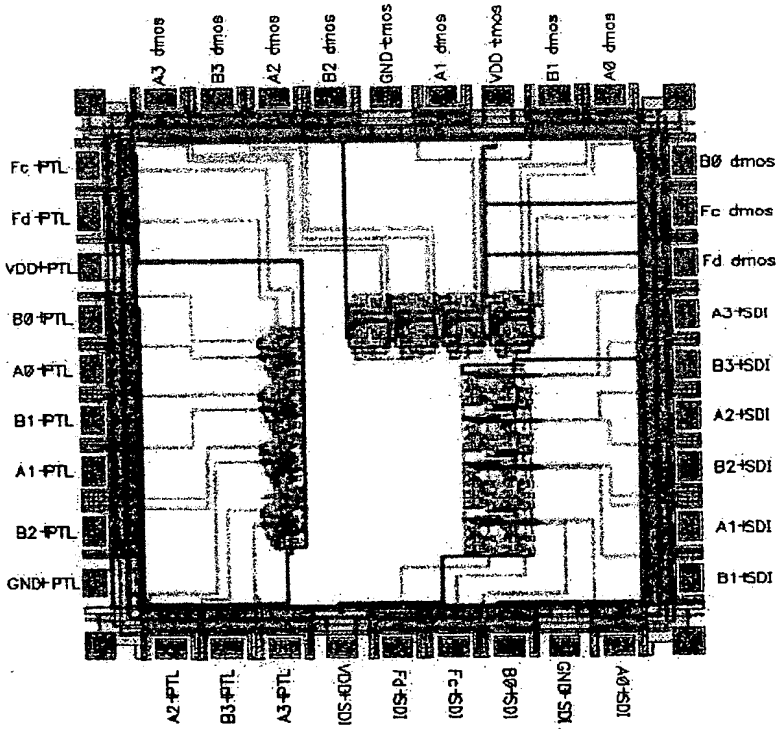

A3 dmos
B3 dmos
A2 dmos
B2 dmos
GND dmos
A1 dmos
VDD dmos
B1 dmos
A0 dmos
Fc PTL
Fd PTL
VDD PTL
B0 PTL
A0 PTL
B1 PTL
A1 PTL
B2 PTL
GND PTL
B0 dmos
Fc dmos
Fd dmos
A3 SDI
B3 SDI
A2 SDI
B2 SDI
A1 SDI
B1 SDI
A2 PTL
B3 PTL
A3 PTL
VDD SDI
Fd SDI
Fc SDI
B0 SDI
GND SDI
A0 SDI

Fig. 27

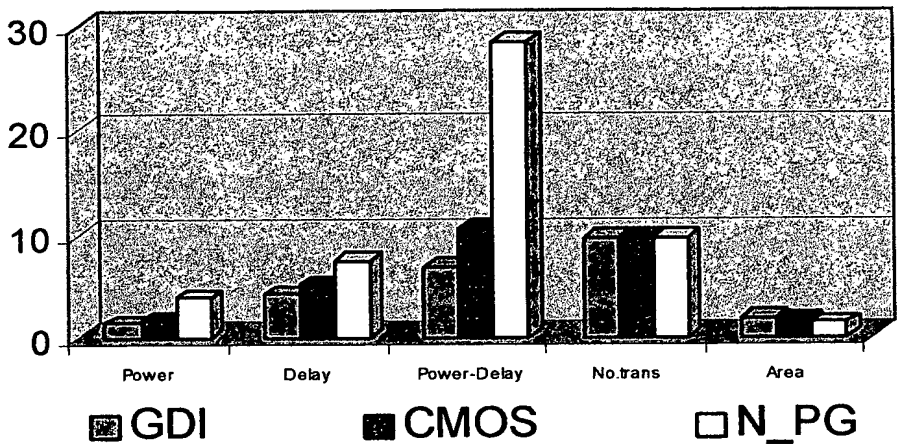


Fig. 28

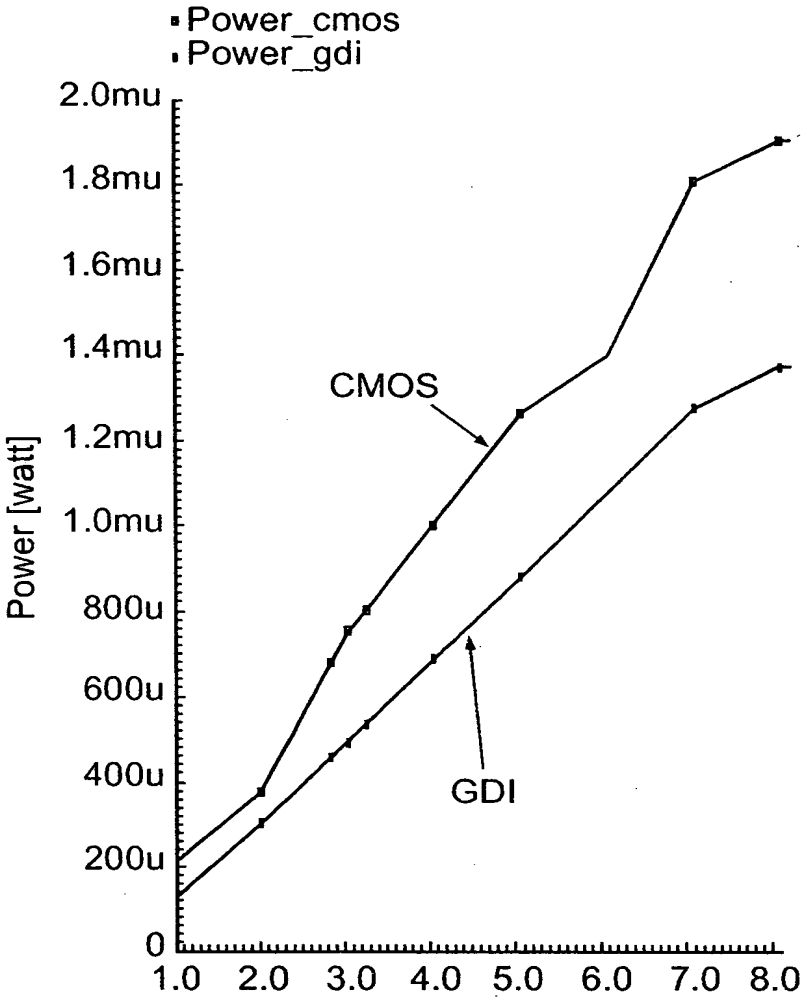

Power_cmos
Power_gdi
2.0mu
1.8mu
1.6mu
1.4mu
1.2mu
1.0mu
800u
600u
400u
200u
0
Power [watt]
CMOS
GDI
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0

Fig. 29

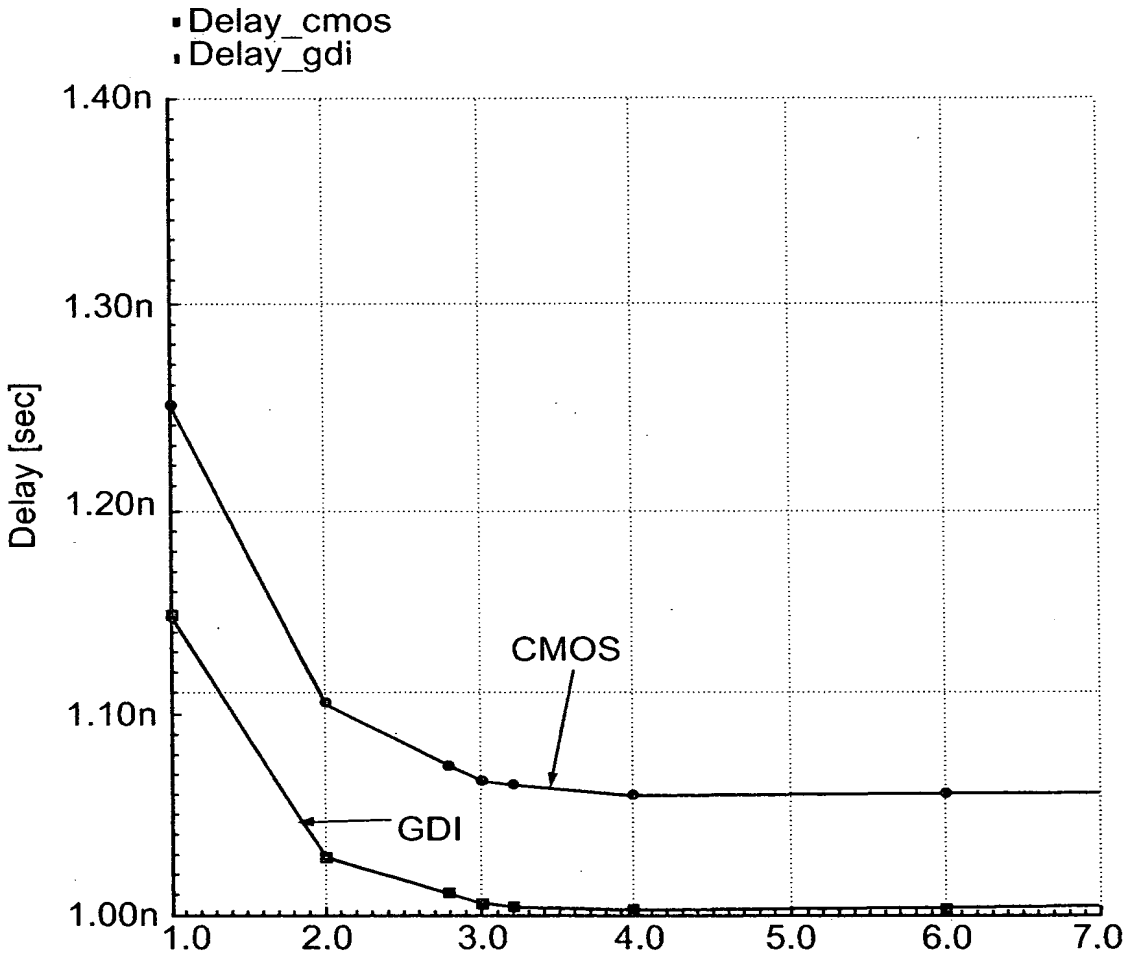

Delay_cmos
Delay_gdi
1.40n
1.30n
1.20n
1.10n
1.00n
Delay [sec]
CMOS
GDI
1.0
2.0
3.0
4.0
5.0
6.0
7.0

Fig. 30

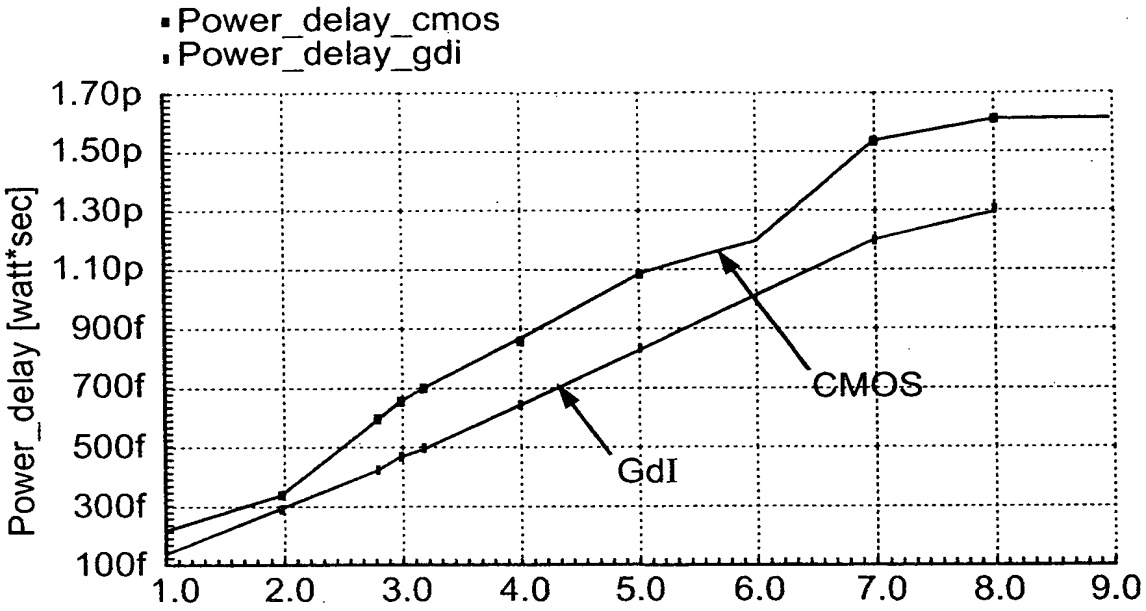

Power_delay_cmos
Power_delay_gdi
1.70p
1.50p
1.30p
1.10p
900f
700f
500f
300f
100f
Power_delay [watt*sec]
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
CMOS
GdI

Fig. 31

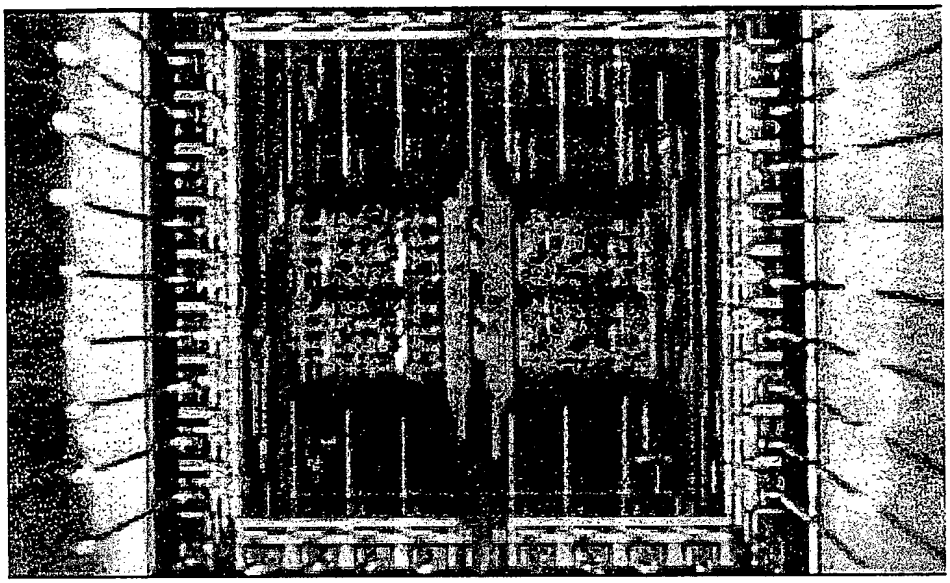


Fig. 32

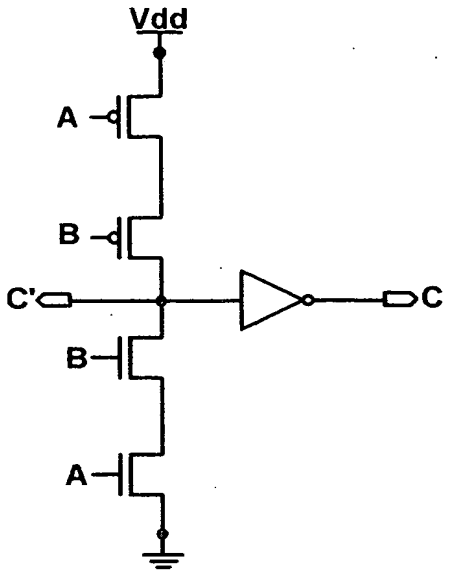


Fig. 33a - Prior art

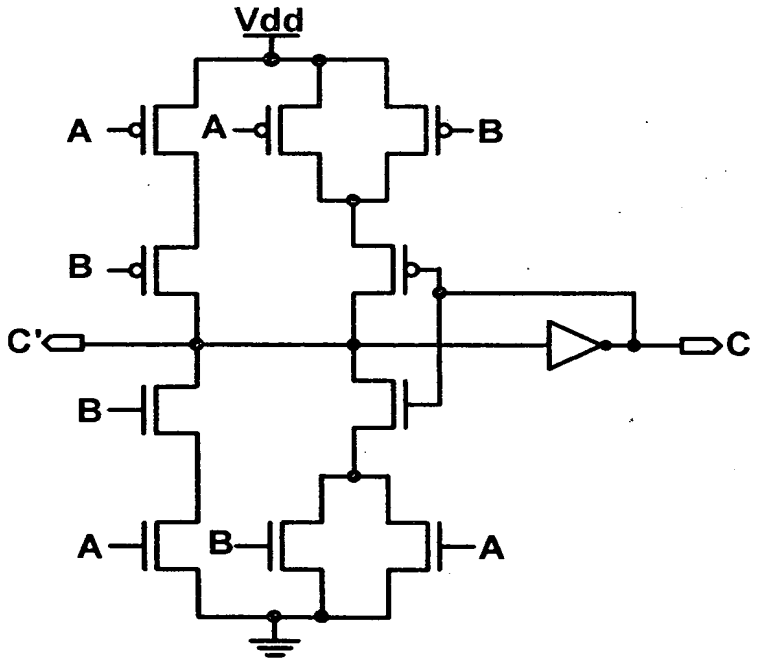


Fig. 33b - Prior art

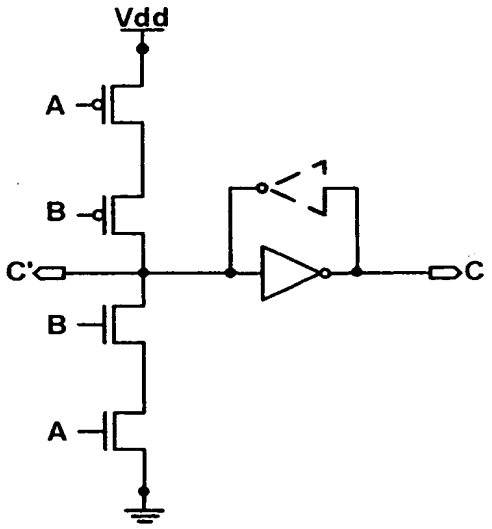


Fig. 33c - Prior art

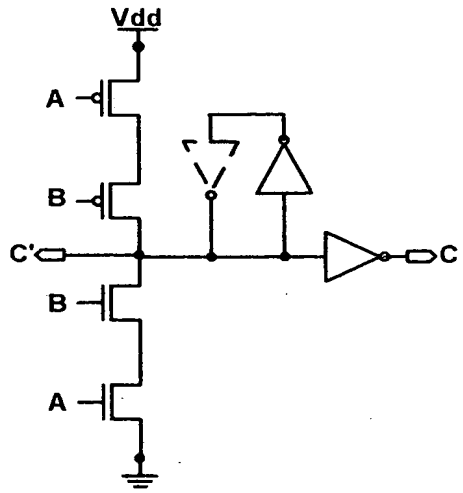


Fig. 33d - Prior art

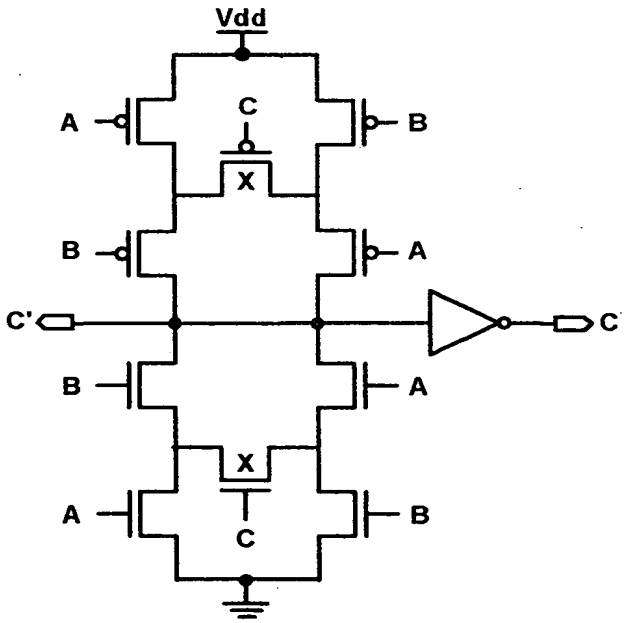


Fig. 33e - Prior art

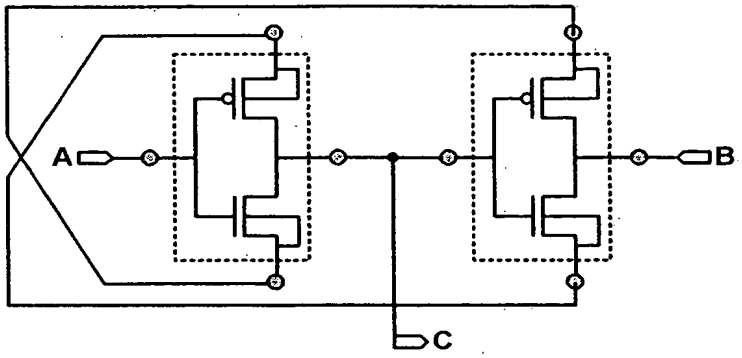


Fig. 34a

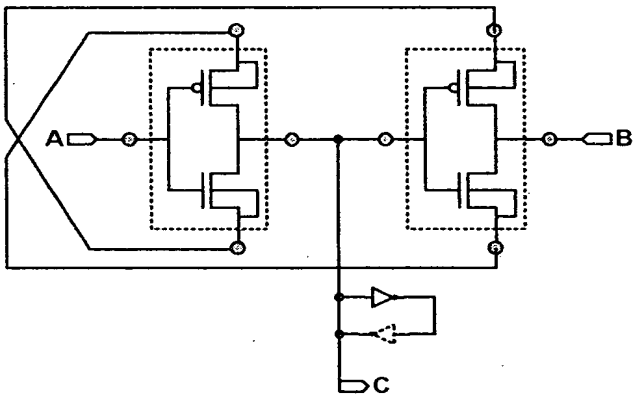


Fig. 34b

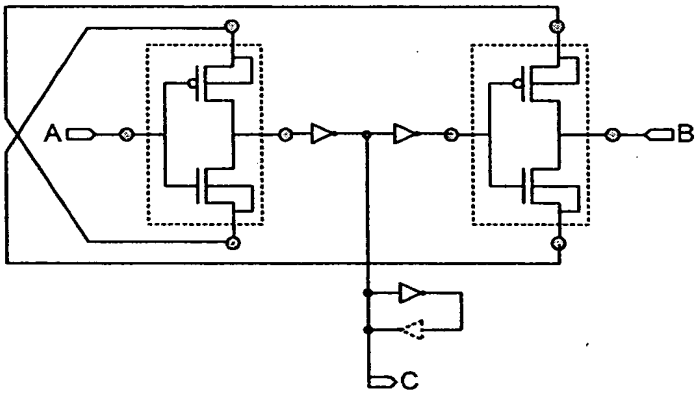


Fig. 34c

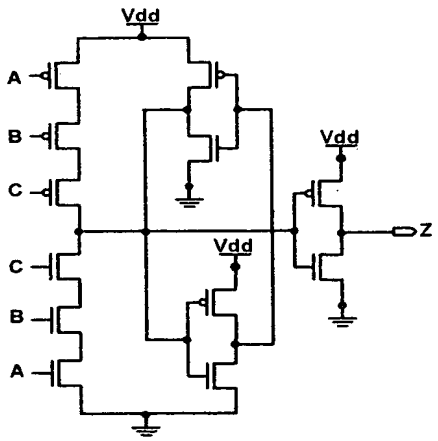


Fig. 35a CMOS – Prior art

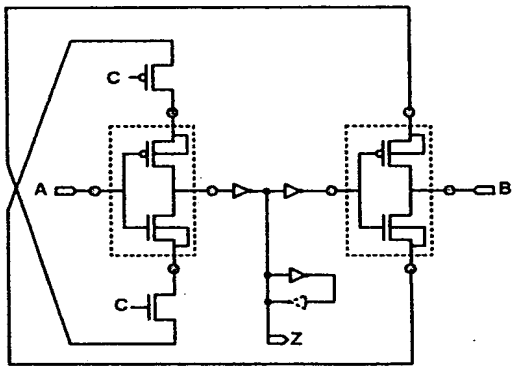


Fig. 35b GDI

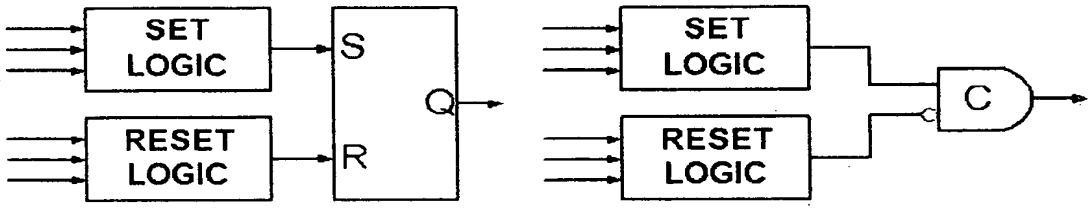


Fig. 36 – Prior art

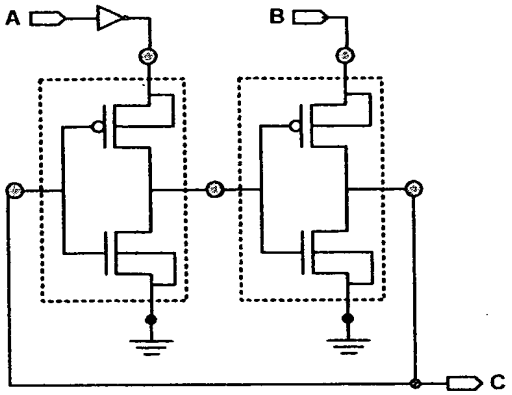


Fig. 37a

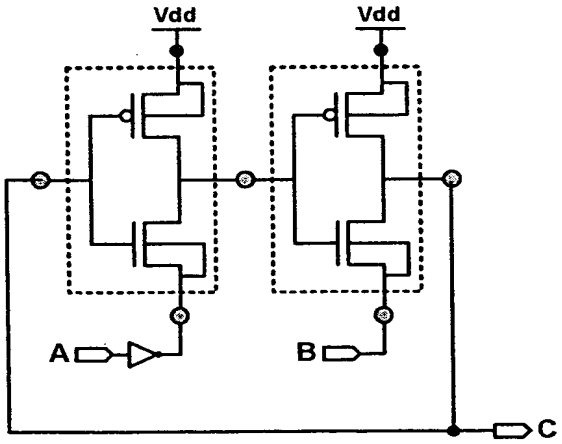


Fig. 37b

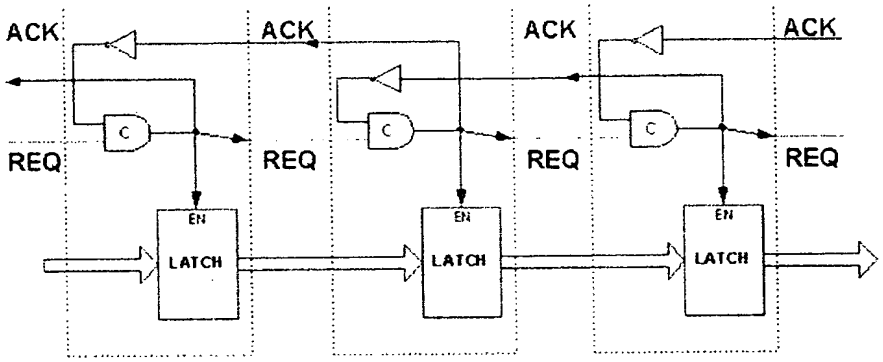


Fig. 38 – Prior art

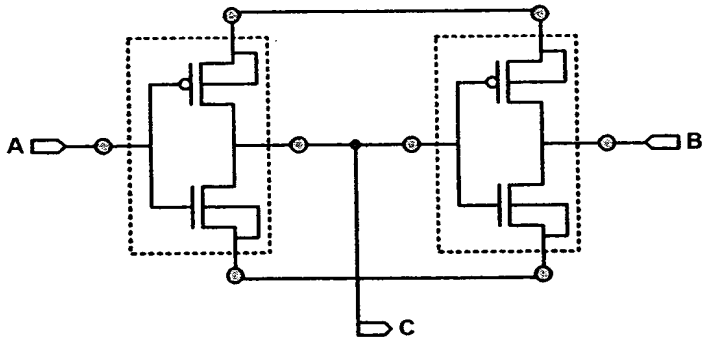


Fig. 39

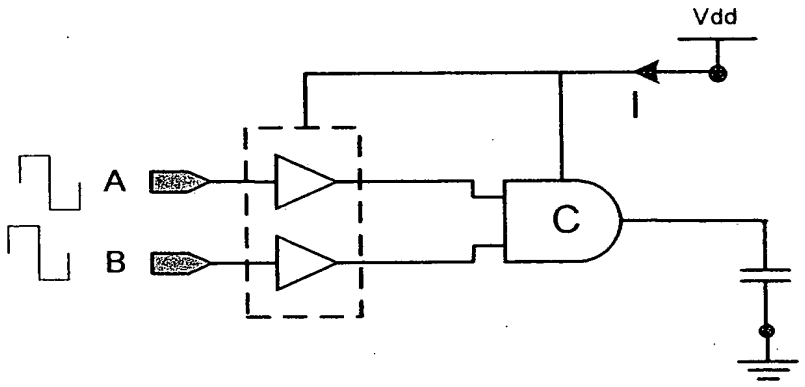


Fig. 40

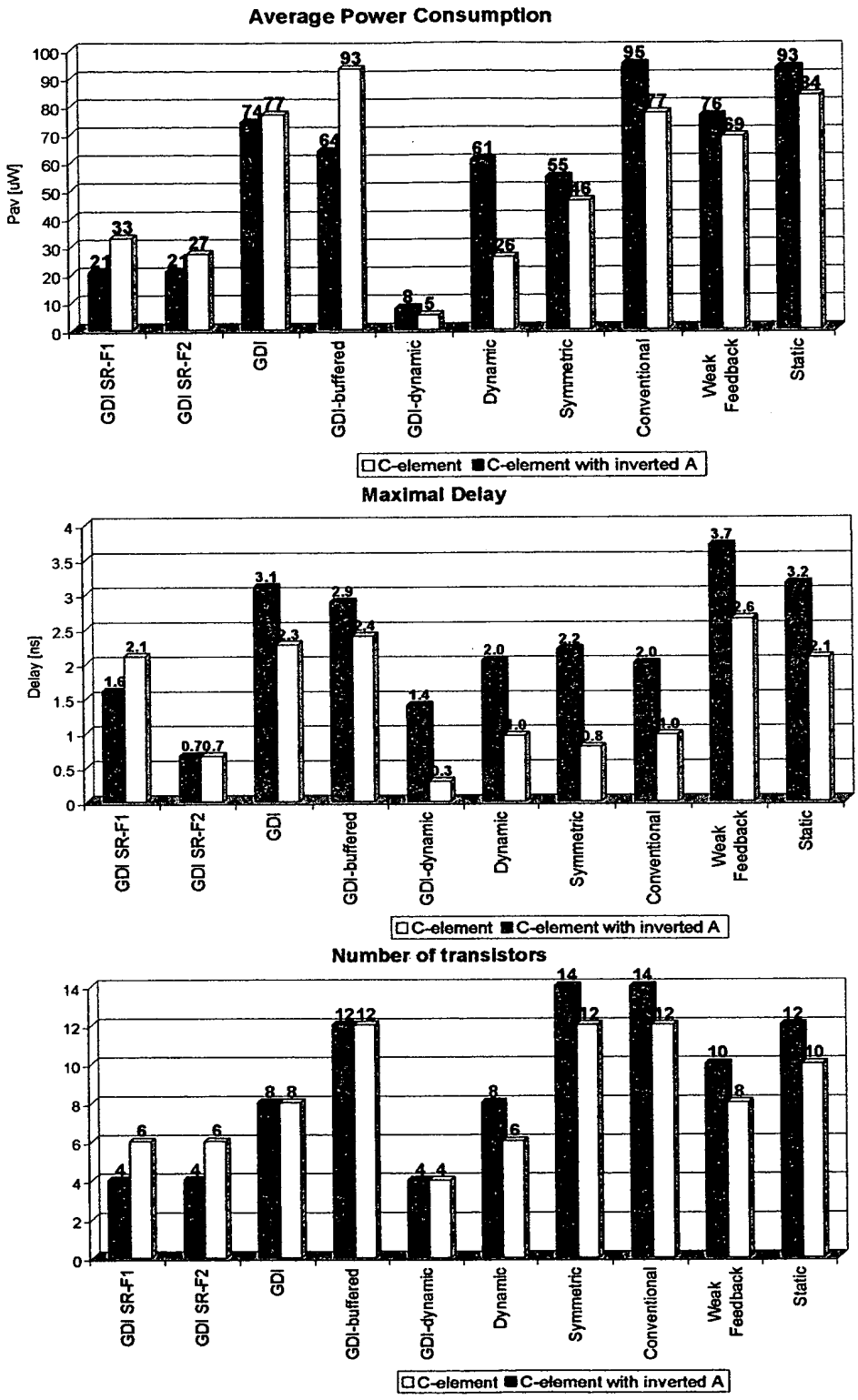

Average Power Consumption
Pav [uW]
100
90
80
70
60
50
40
30
20
10
0
21
33
21
27
74
77
64
93
8
5
61
26
55
46
95
77
76
69
93
84
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A
Maximal Delay
Delay [ns]
4
3.5
3
2.5
2
1.5
1
0.5
0
1.6
2.1
0.7
0.7
3.1
2.3
2.9
2.4
1.4
0.3
2.0
1.0
2.2
0.8
2.0
1.0
3.7
2.6
3.2
2.1
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A
Number of transistors
14
12
10
8
6
4
2
0
4
6
4
6
8
8
12
12
4
4
8
6
14
12
14
12
10
8
12
10
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A

Fig. 41

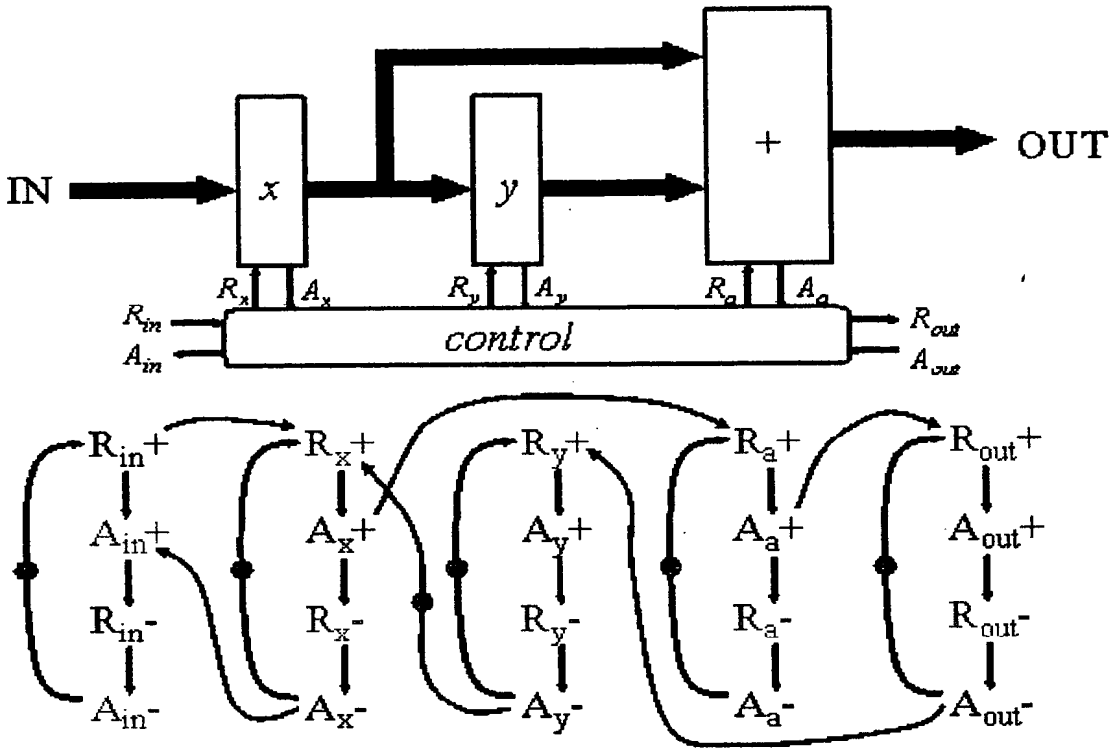


Fig. 42 – Prior art

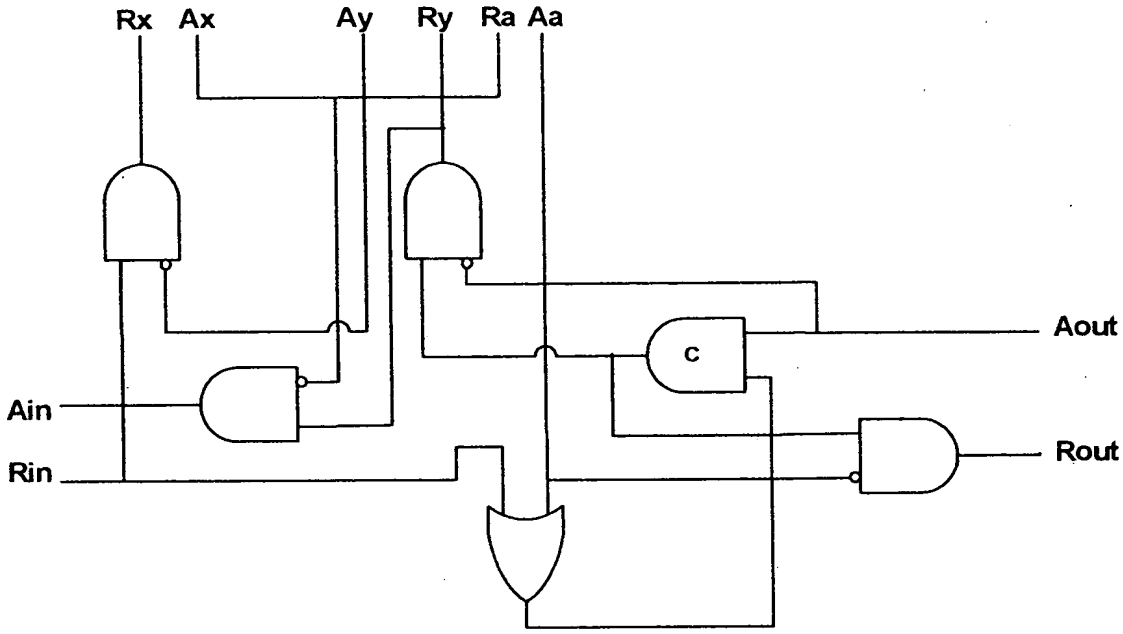


Fig. 43a – Prior art

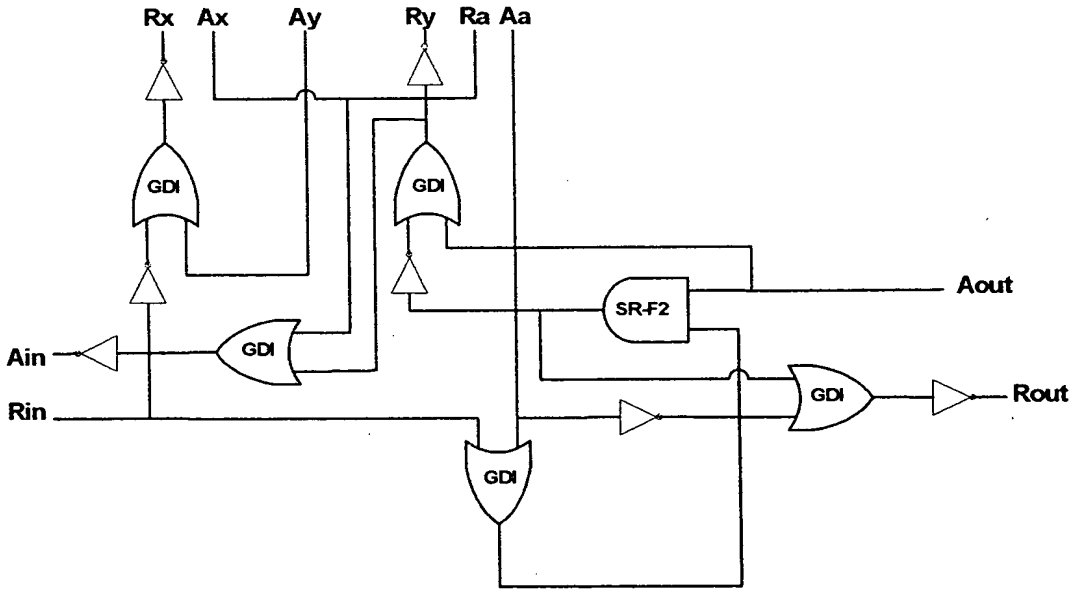


Fig. 43b – Prior art

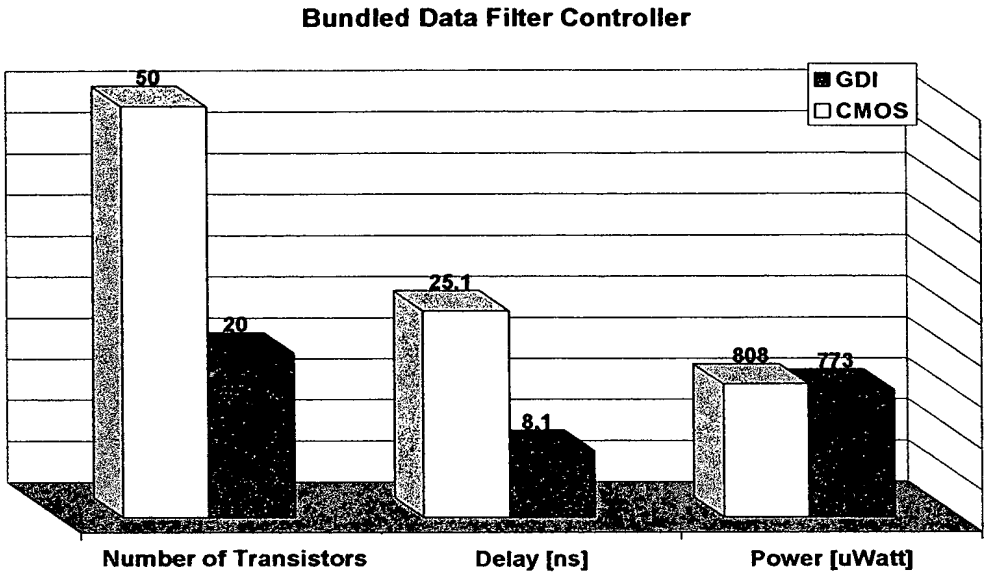

Bundled Data Filter Controller
GDI
CMOS
50
20
25.1
8.1
808
773
Number of Transistors
Delay [ns]
Power [uWatt]

Fig. 44

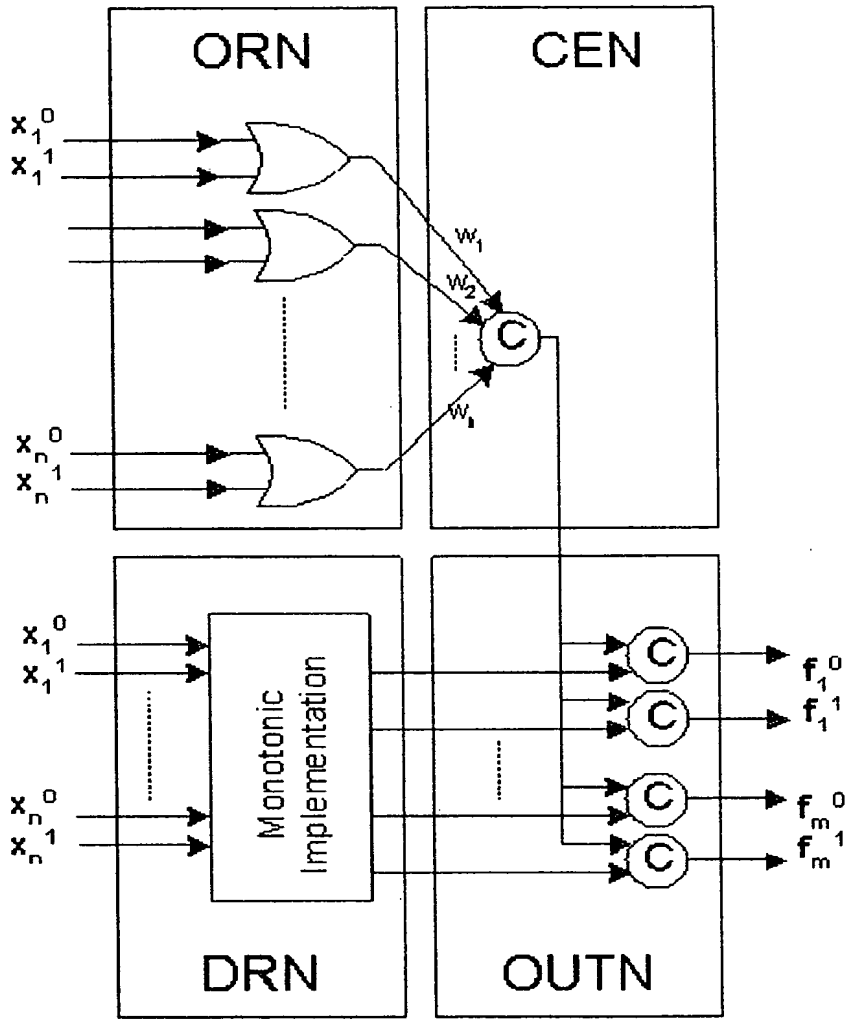
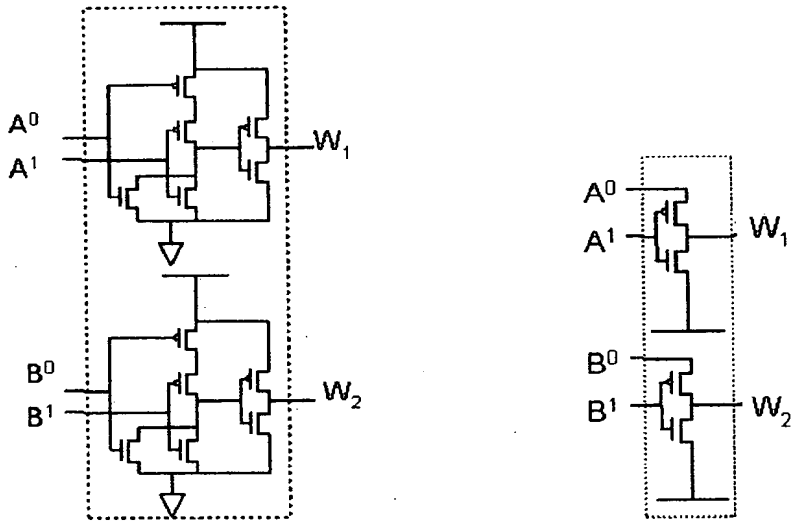
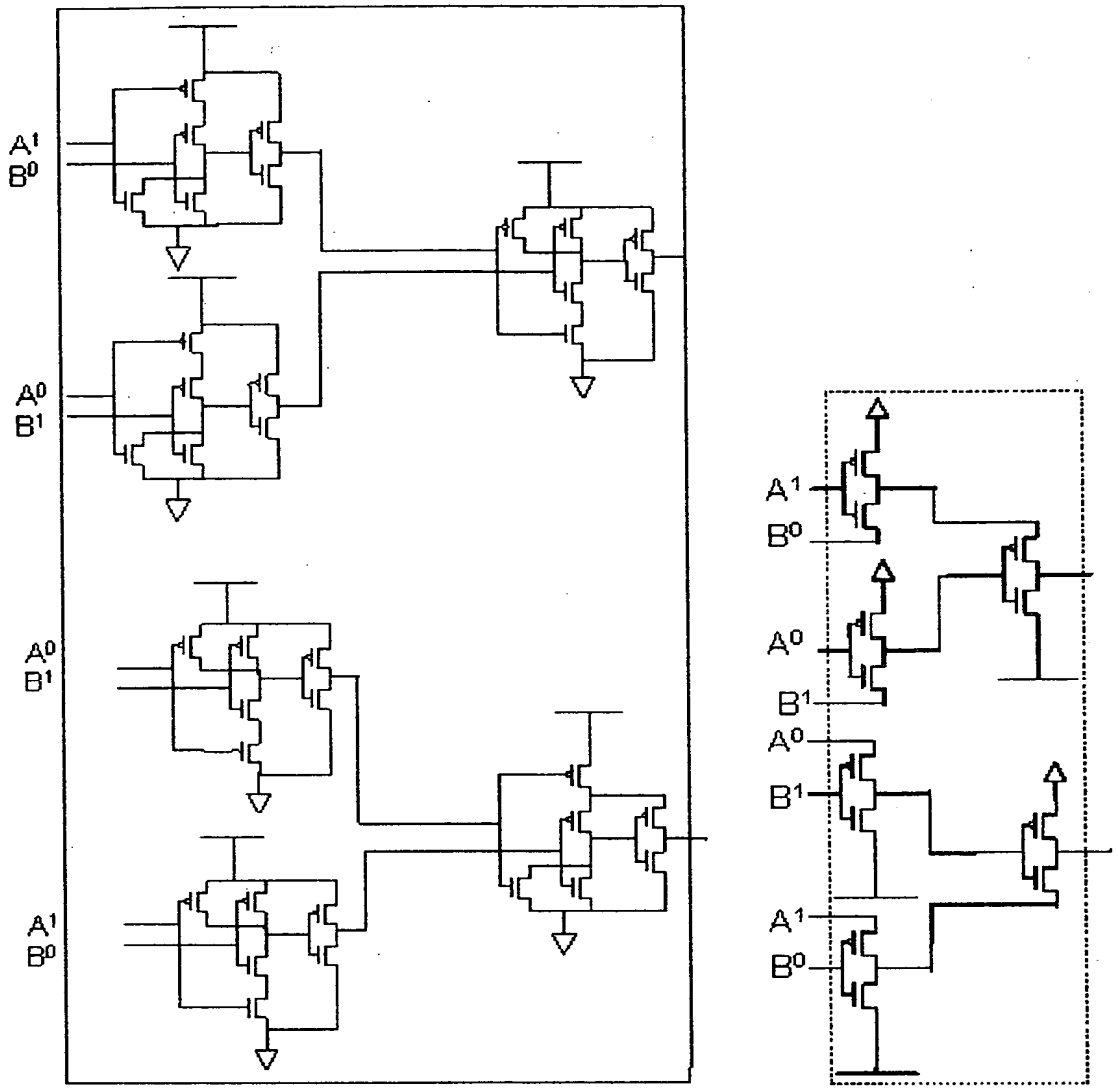


Fig. 45 – Prior art



CMOS - Prior art **GDI**

Fig. 46



CMOS - Prior art **GDI**

Fig. 47

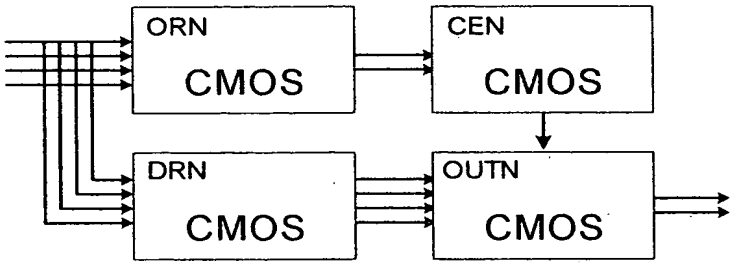


Fig. 48a

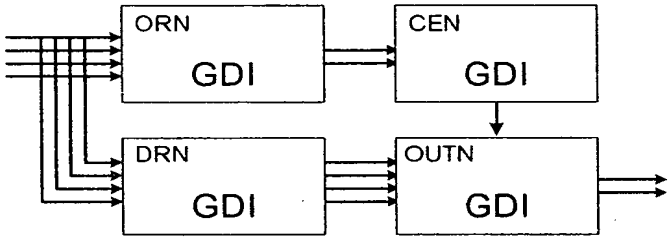


Fig. 48b

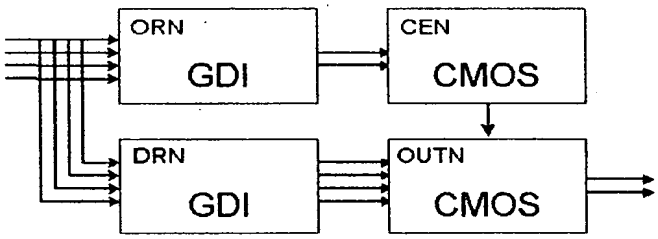


Fig. 48c

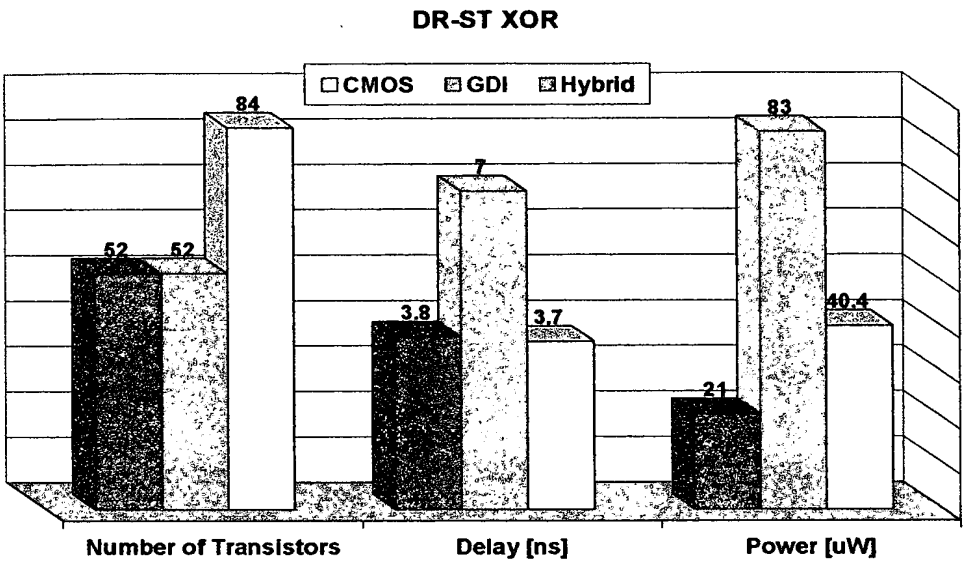
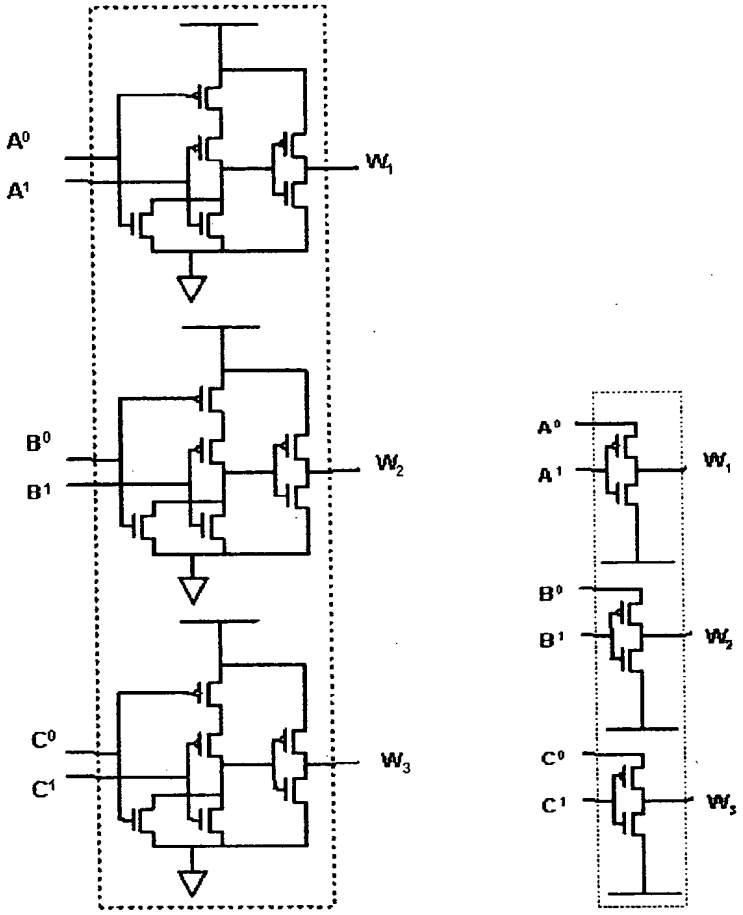

DR-ST XOR
CMOS
GDI
Hybrid
52
52
84
3.8
7
3.7
21
83
40.4
Number of Transistors
Delay [ns]
Power [uW]

Fig. 49



CMOS - Prior art **GDI**

Fig. 50

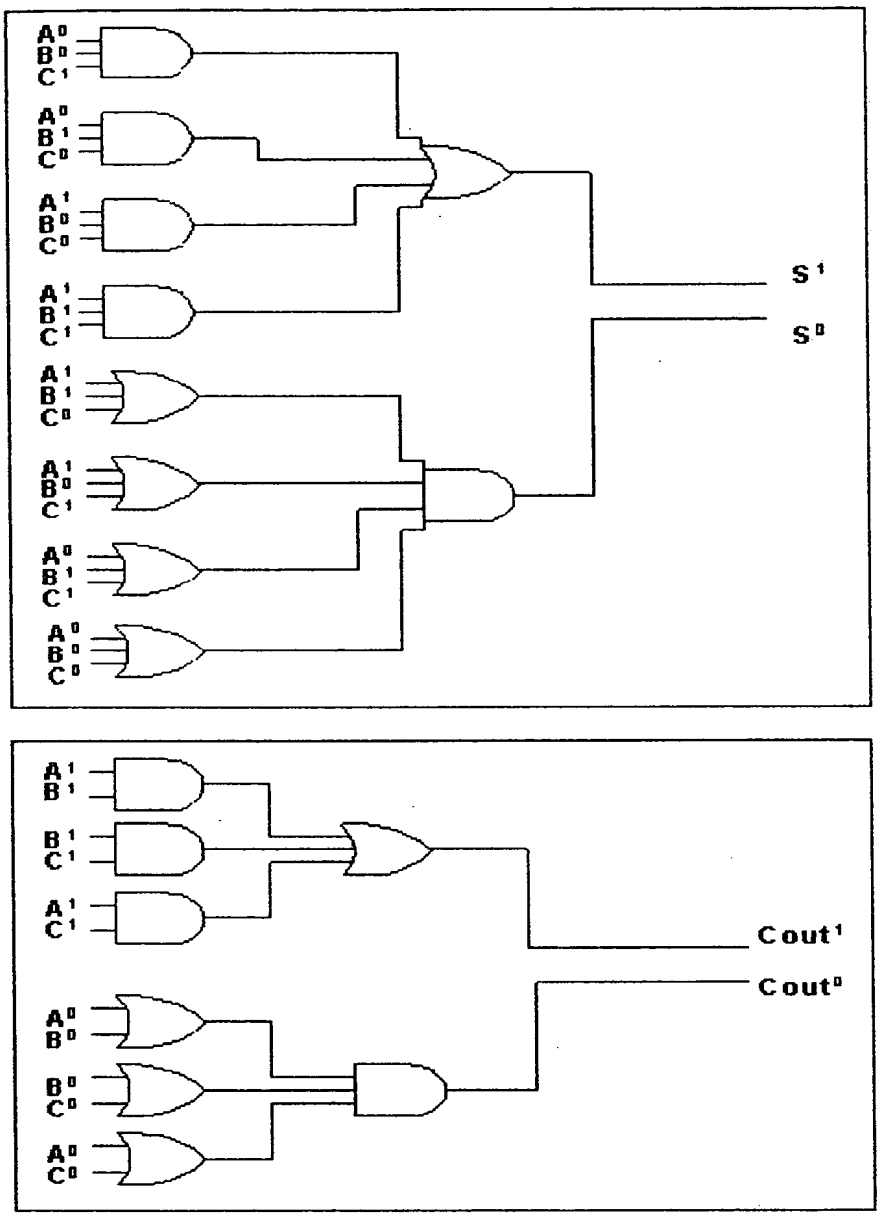


Fig. 51 – Prior art

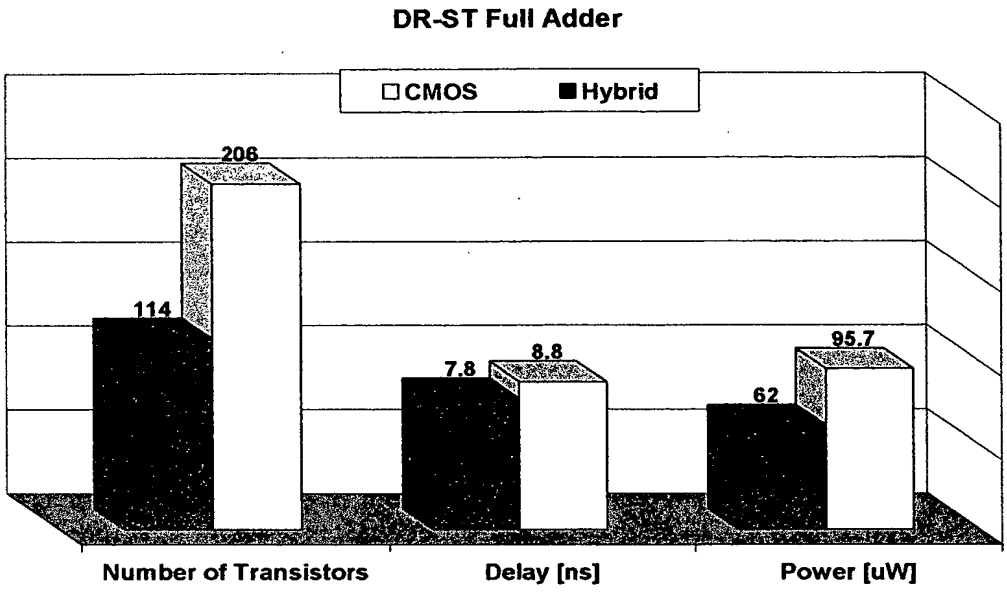

DR-ST Full Adder
CMOS
Hybrid
206
114
7.8
8.8
62
95.7
Number of Transistors
Delay [ns]
Power [uW]

Fig. 52

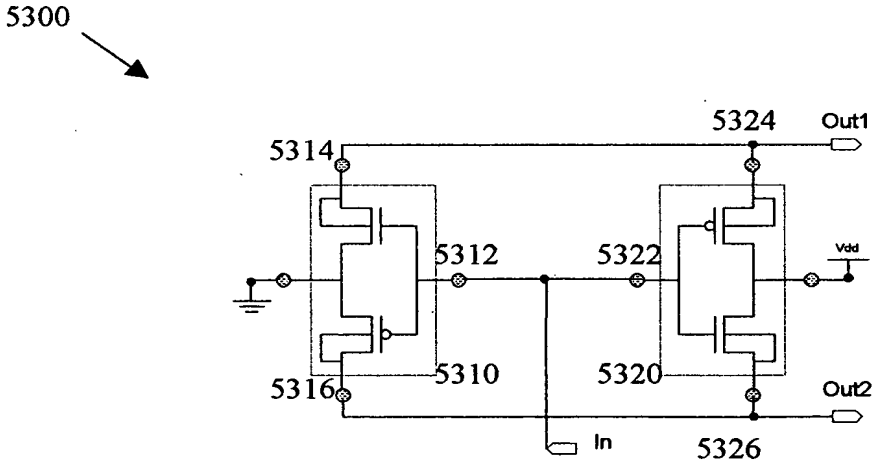

5300
5324
Out1
5314
5312
5322
Vdd
5310
5320
5316
Out2
In
5326

Fig. 53